2013 S-Series Intel Shark Bay

UMA/DIS Muxless Schematic
14.0"Rampage 15.6"Renegade 17.0"Ricochet

Haswell-M Dual/Quad Core SV
rPGA947 37W
Lynx Point-M PCH

www.aitech1.ru

REV:MV

2013-08-01

DY:No stuff
DIS_PX:Only DIS install

<Core Design>

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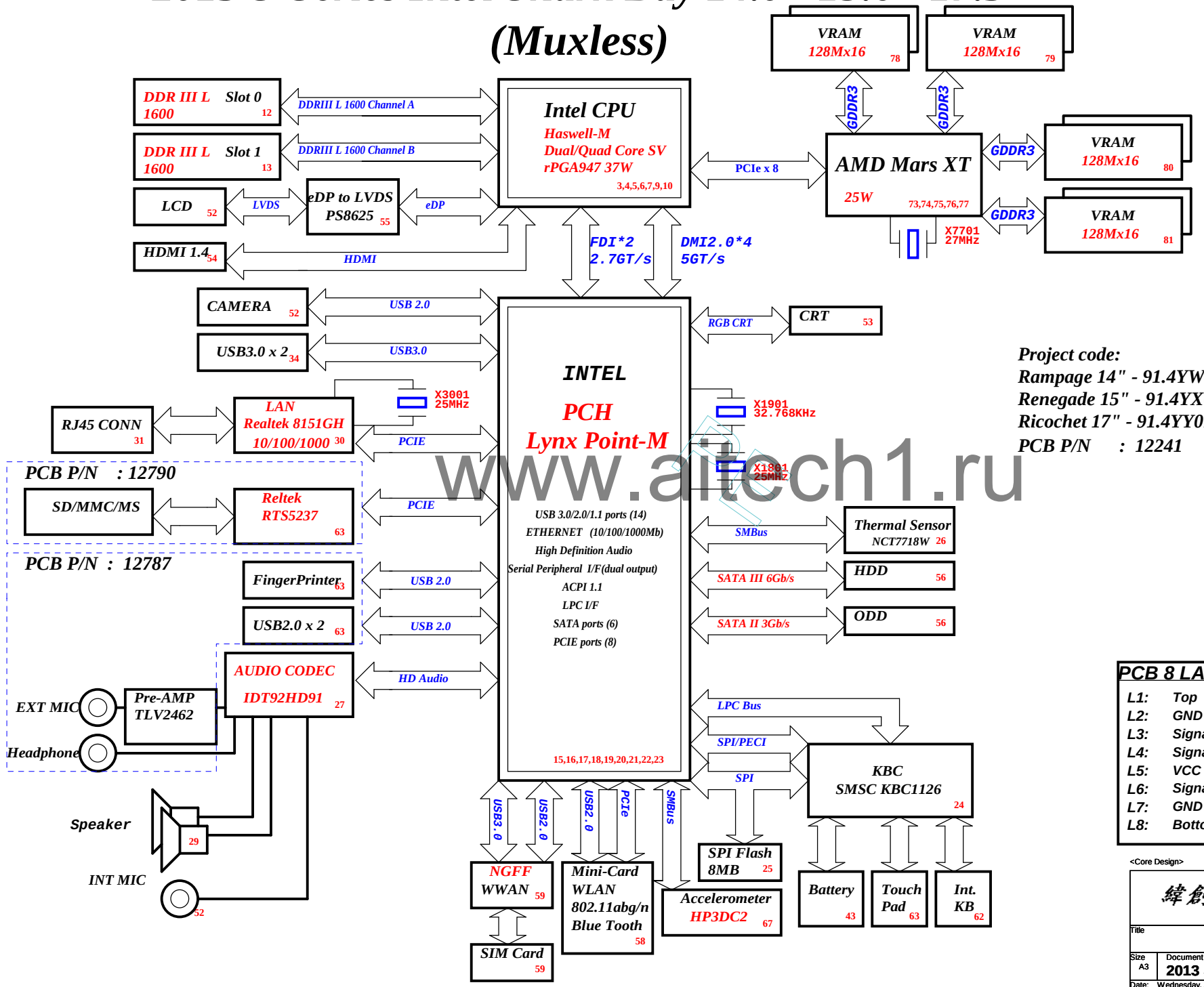
Title	Cover Page	
Size A4	Document Number 2013 S-Series Shark Bay 14 15 17	Rev 1
Date: Thursday, August 01, 2013	Sheet 1 of 103	

2013 S-Series Intel Shark Bay 14.0" 15.6" 17.3" (Muxless)



Project code:
Rampage 14" - 91.4YW01.001
Renegade 15" - 91.4YX01.001
Ricochet 17" - 91.4YY01.001
PCB P/N : 12241

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CPU DC/DC TPS51631RSMR 46,47

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS51367RVER 48

INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC RT8223MZQW 45

INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC TPS51216RUKR 49

INPUTS	OUTPUTS
DCBATOUT	1D35V_S3 0D675V_S0 DDR_VREF_S3

SYSTEM DC/DC APL5930KAI 51

INPUTS	OUTPUTS
3D3V_S5	1D5V_S0

VGA ADP3211MNR2G 82

INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

CHARGER BQ24736RGRR 44

INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

VGA G9661-25ADJF11U 83

INPUTS	OUTPUTS
3D3V_S0	1D8V_VGA_S0

VGA APL5930KAI 83

INPUTS	OUTPUTS
1D35V_S3	0D95V_VGA_S0

Switches 36,83

INPUTS	OUTPUTS
5V_S5 3D3V_S5 3D3V_S0	5V_S0 3D3V_S0 3D3V_VGA

VGA TPS51211DSCR

INPUTS	OUTPUTS
DCBATOUT	1D5V_VGA_S0 83

PCB 8 LAYER

L1:	Top
L2:	GND
L3:	Signal
L4:	Signal
L5:	VCC
L6:	Signal
L7:	GND
L8:	Bottom

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Title: **Block Diagram**

Size: A3 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

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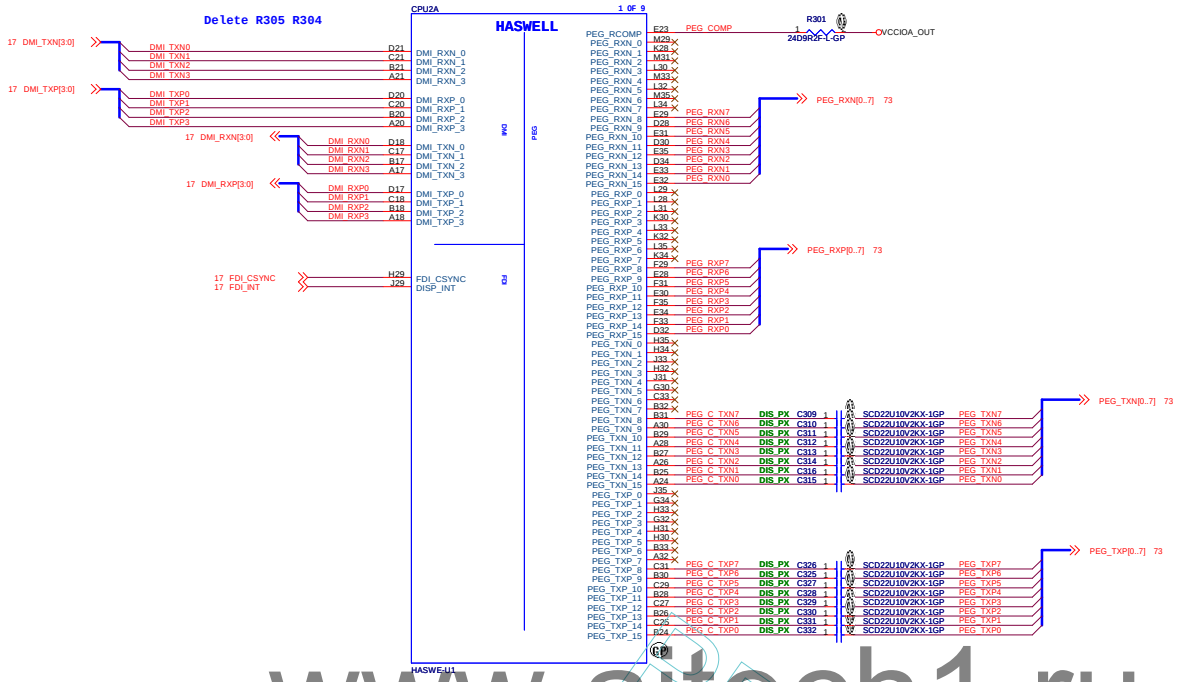
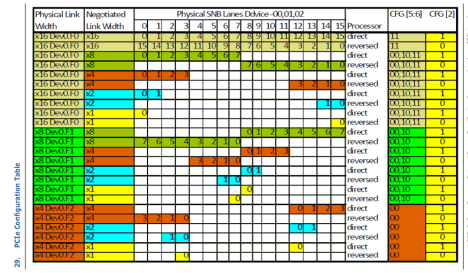
SSID = CPU

Delete R305 R304





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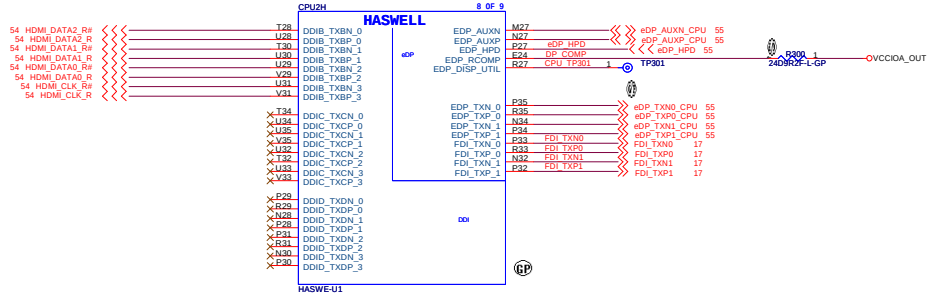
HDMI



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Title: CPU (PCIE/DMI/FDI)

Size	Document Number	Rev
A2	2013 S-Series Shark Bay 14 15 17	1

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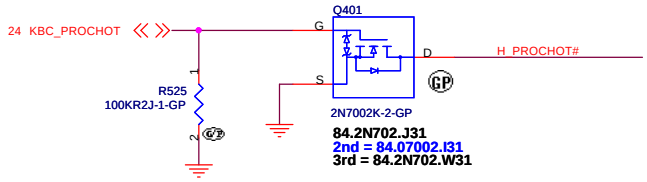
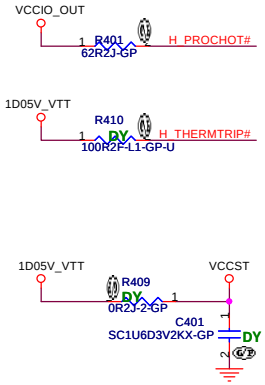
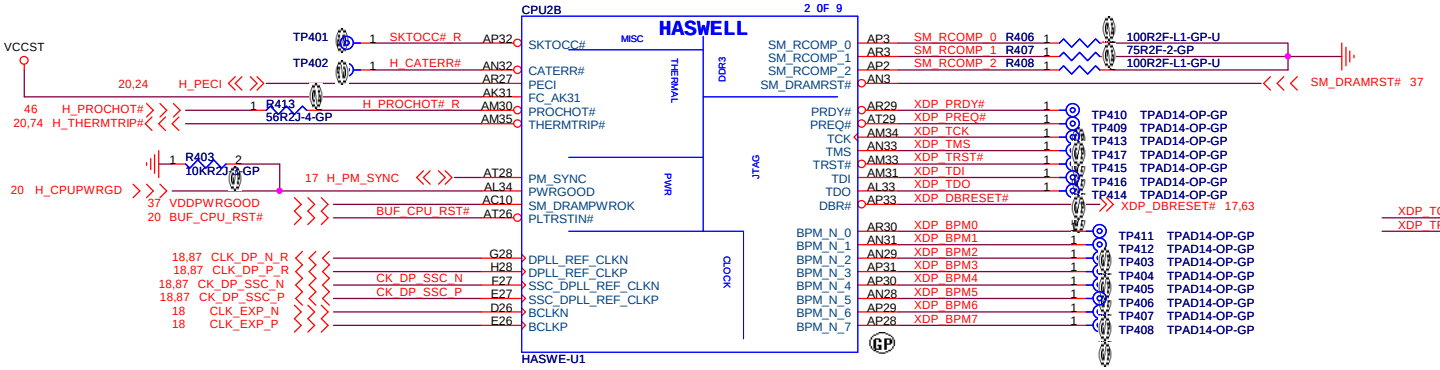
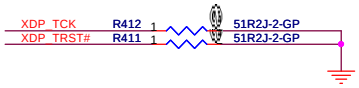
SSID = CPU

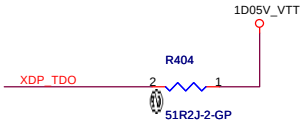


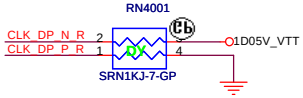
Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.

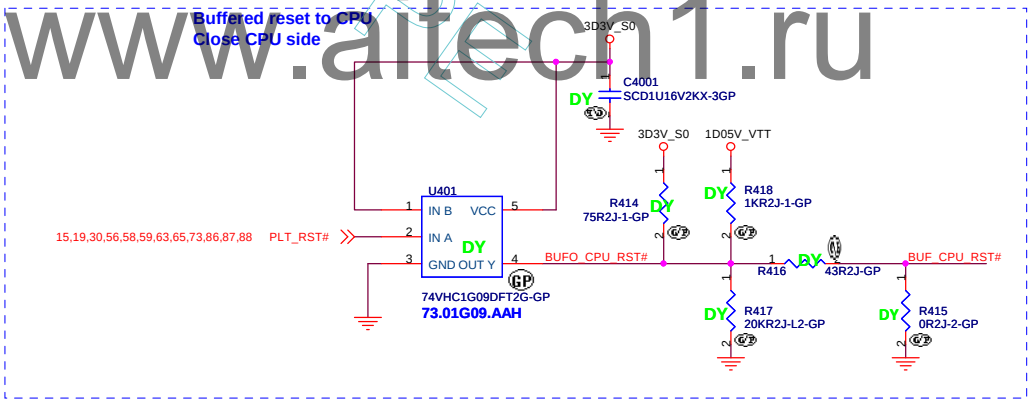












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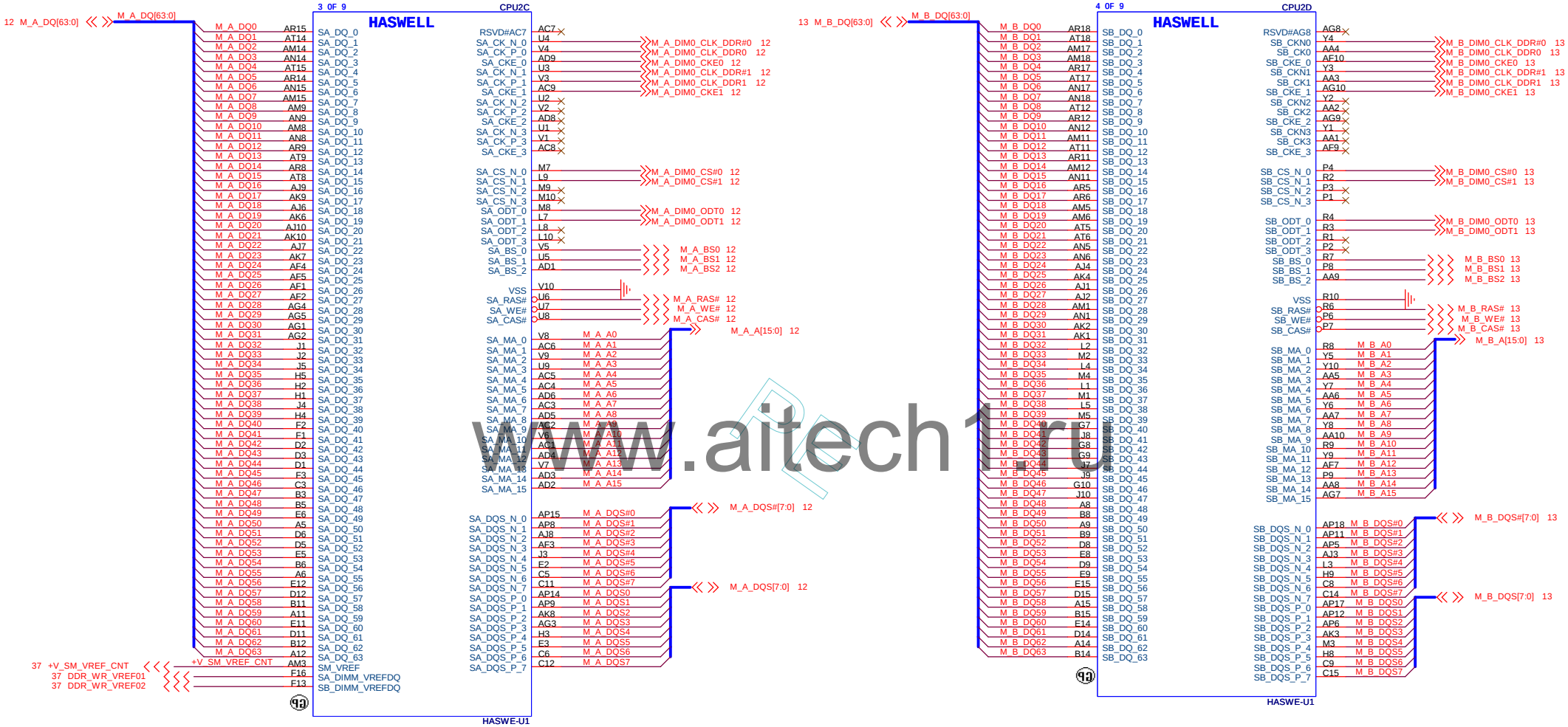
SSID = CPU



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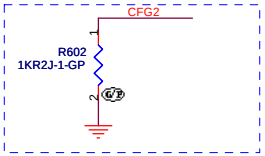
Title: *CPU (DDR)*

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

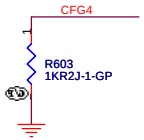
Date: Monday, August 12, 2013 Sheet 5 of 103

SSID = CPU

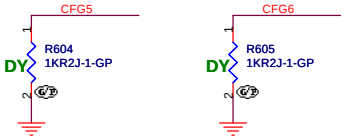
PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed

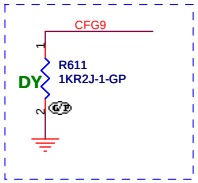


eDP Enable	
CFG4	1:Disable 0:Enable

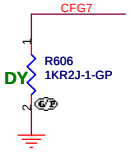


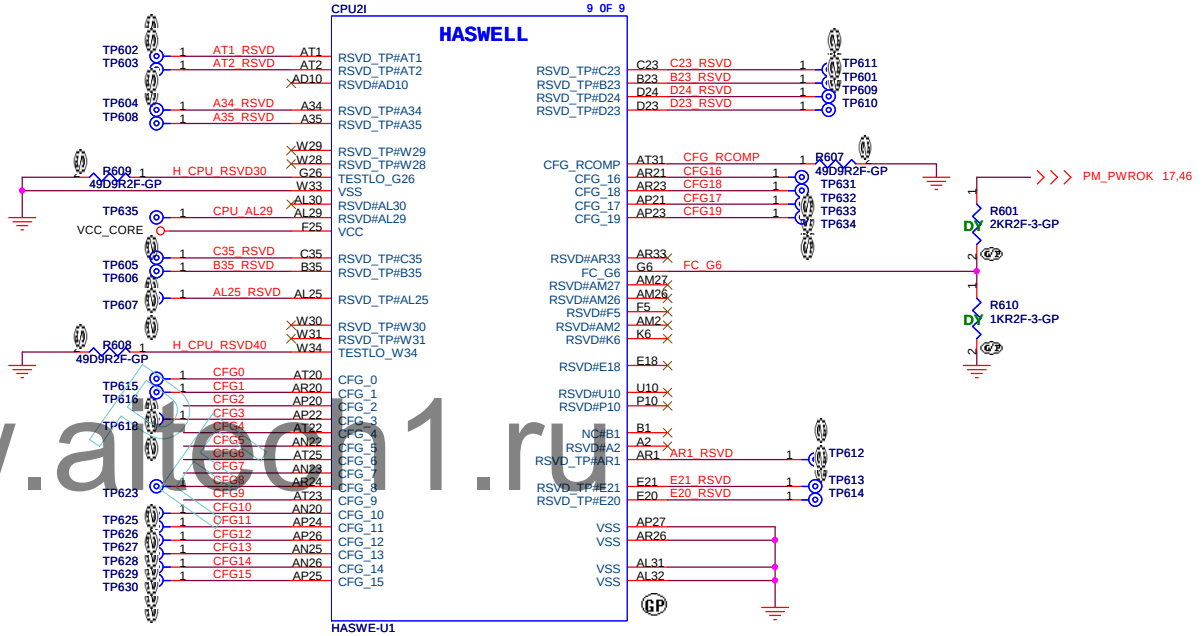
PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled





PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training





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Title: CPU (RESERVED)

Size: A3 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

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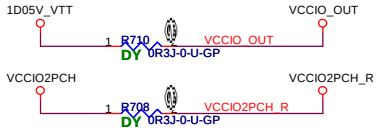
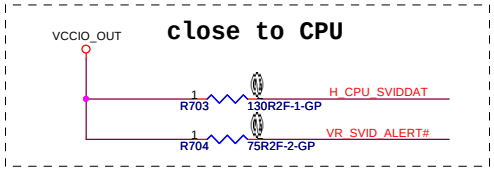
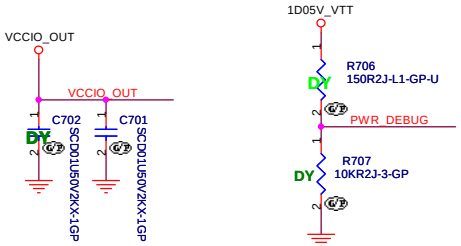
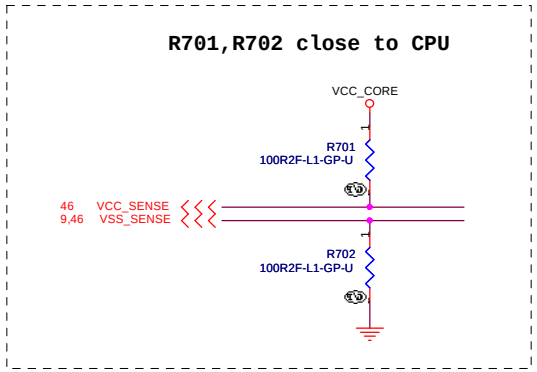
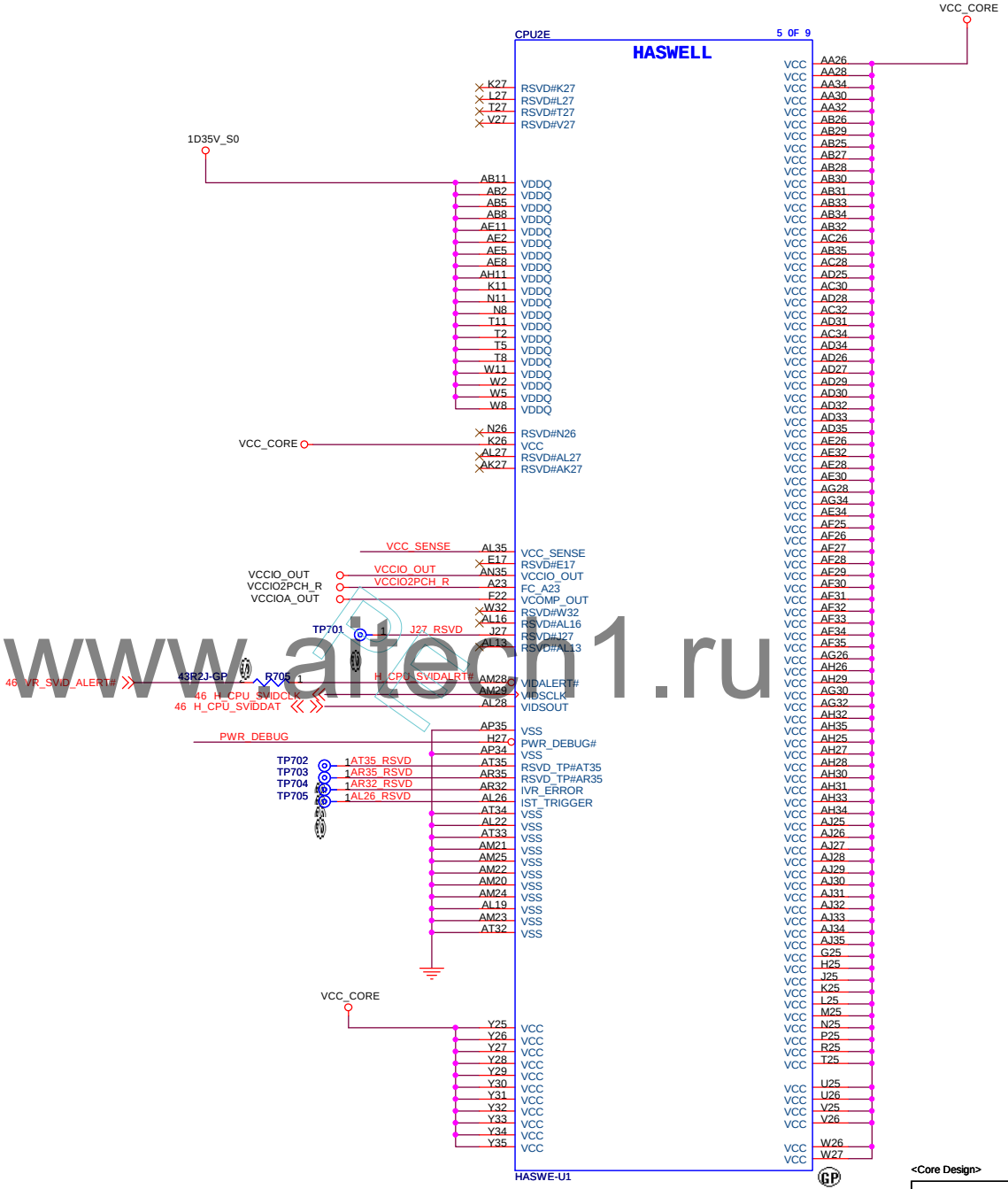
SSID = CPU











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Title: CPU (VCC)

Size: A3 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

Date: Monday, August 12, 2013 | Sheet 7 of 103

(Reserved)

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Title: CPU (DDI/EDP)

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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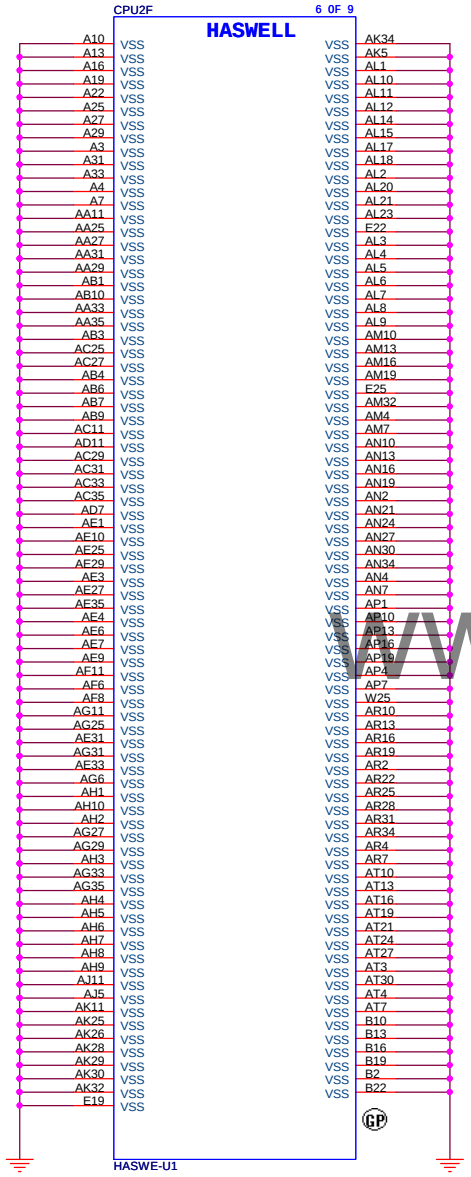
SSID = CPU



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Title: ***CPU (VSS)***

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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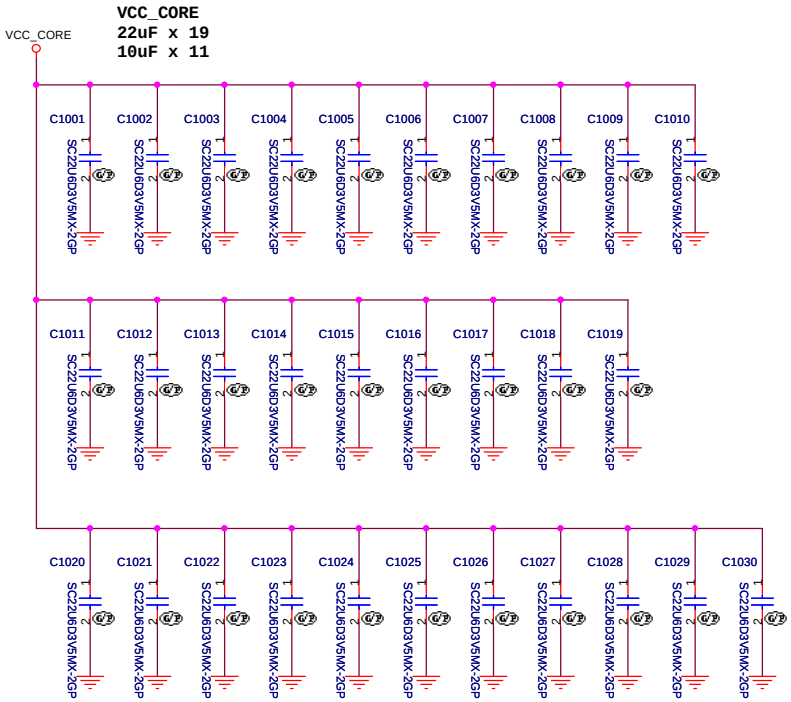

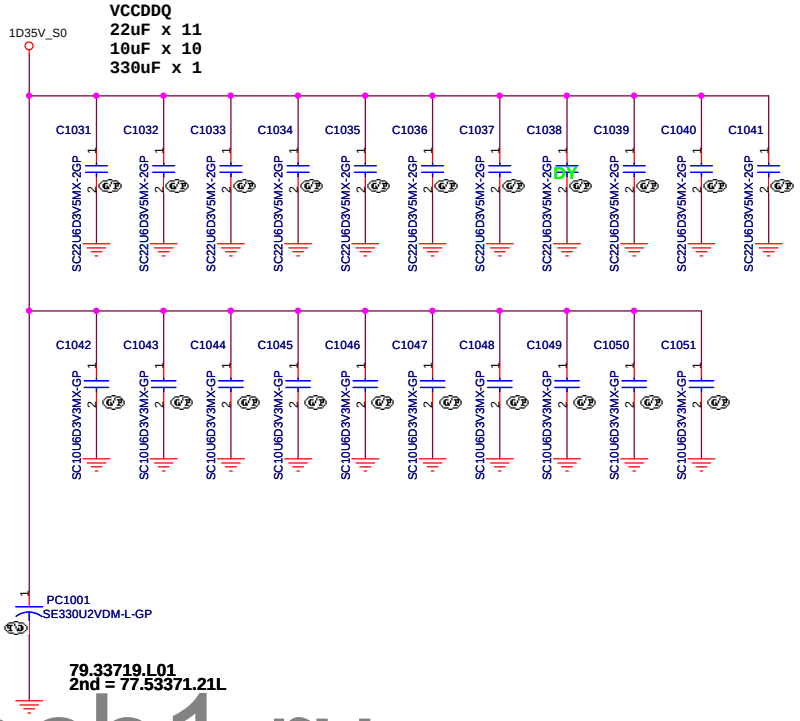

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Title: 010 CPU (Power CAP1)

Size: A3 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

Date: Wednesday, July 03, 2013 | Sheet 10 of 103

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Title: CPU(Power CAP2)

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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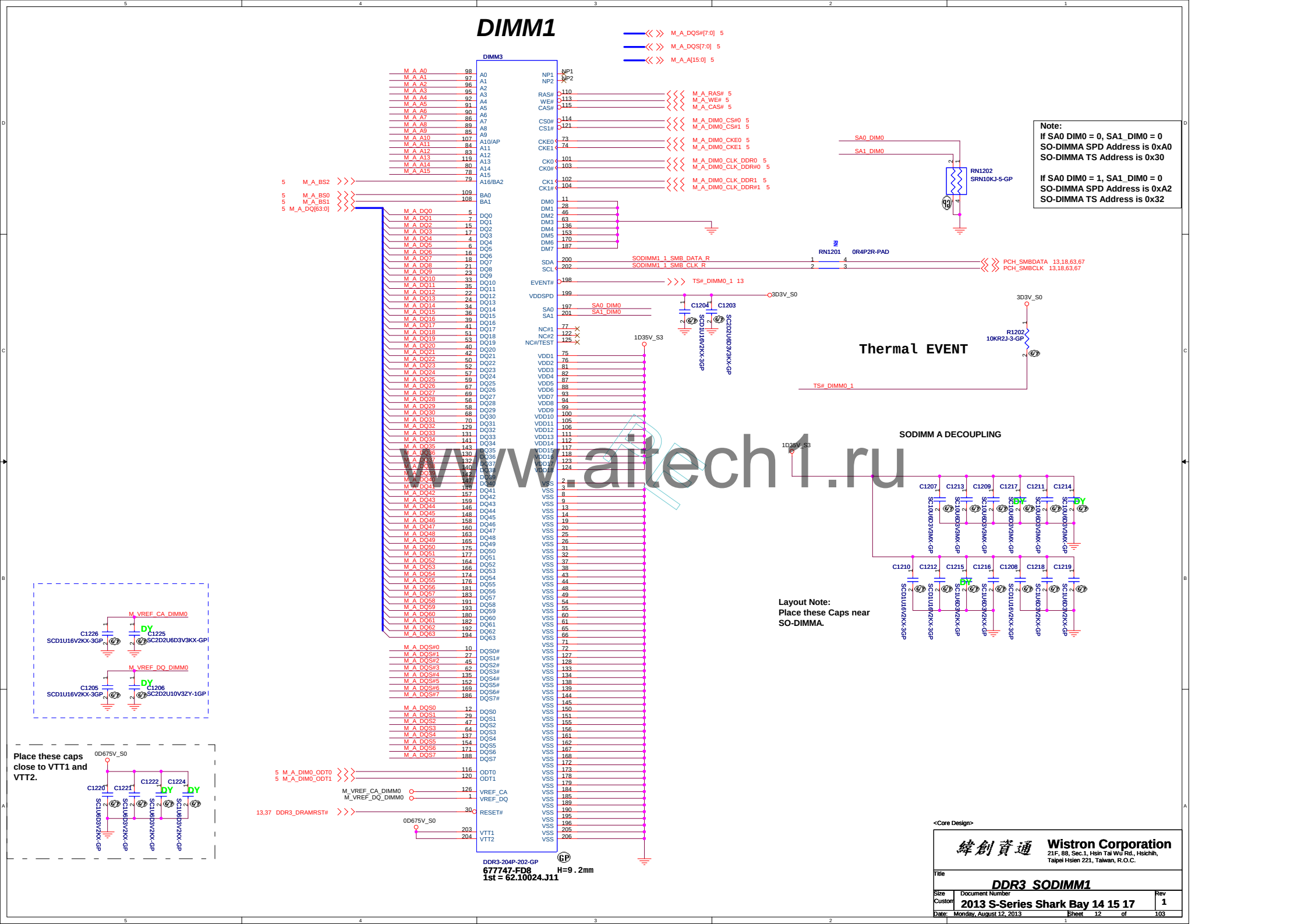
DIMM1



Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

SODIMM A DECOUPLING

Layout Note:
Place these Caps near SO-DIMMA.

Place these caps close to VTT1 and VTT2.

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Title: **DDR3_SODIMM1**

Size	Document Number	Rev
Custom	2013 S-Series Shark Bay 14 15 17	1

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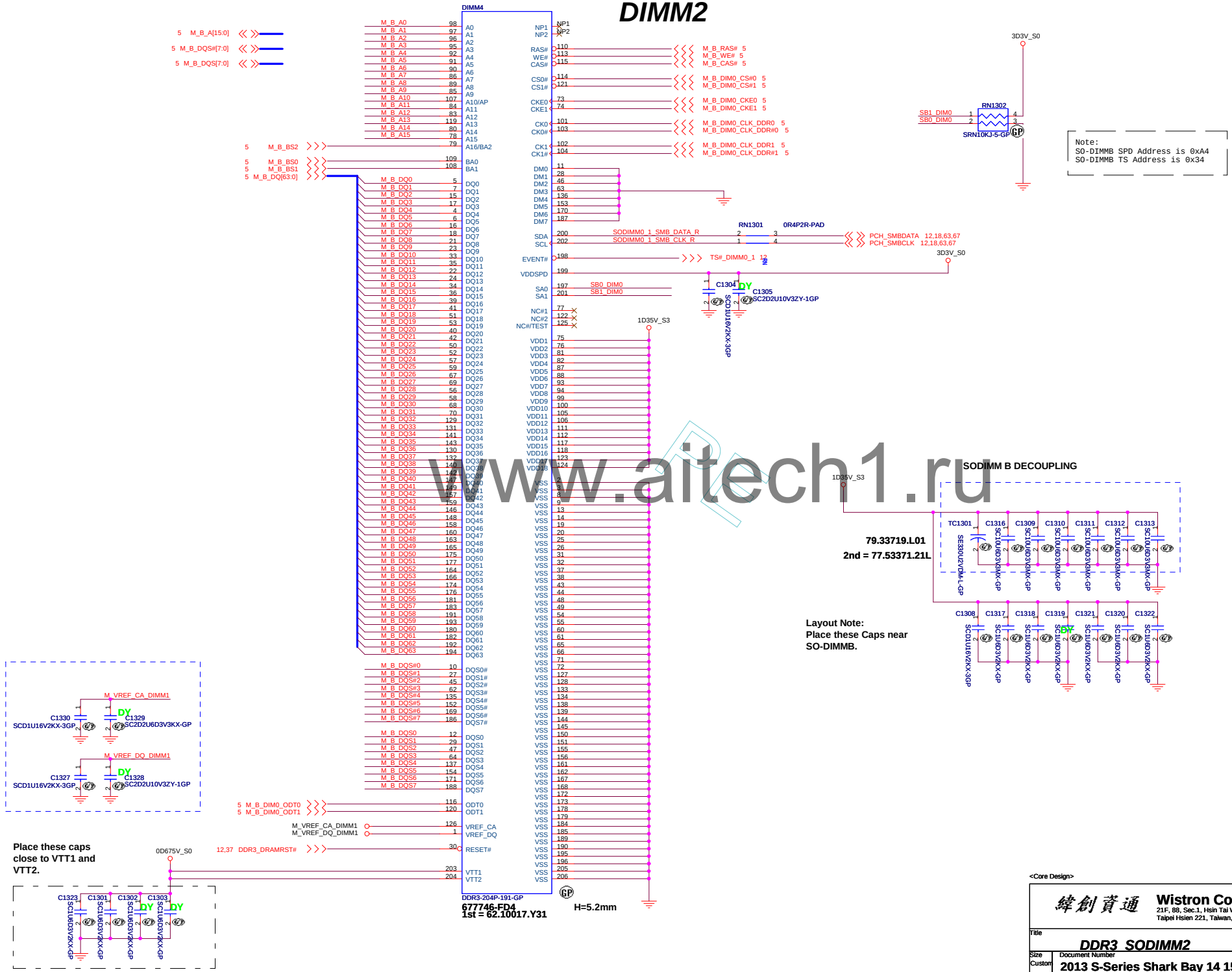
DIMM2



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Title: DDR3_SODIMM2

Size: Custom | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

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Title: ***(Reserved)SODIMM3***

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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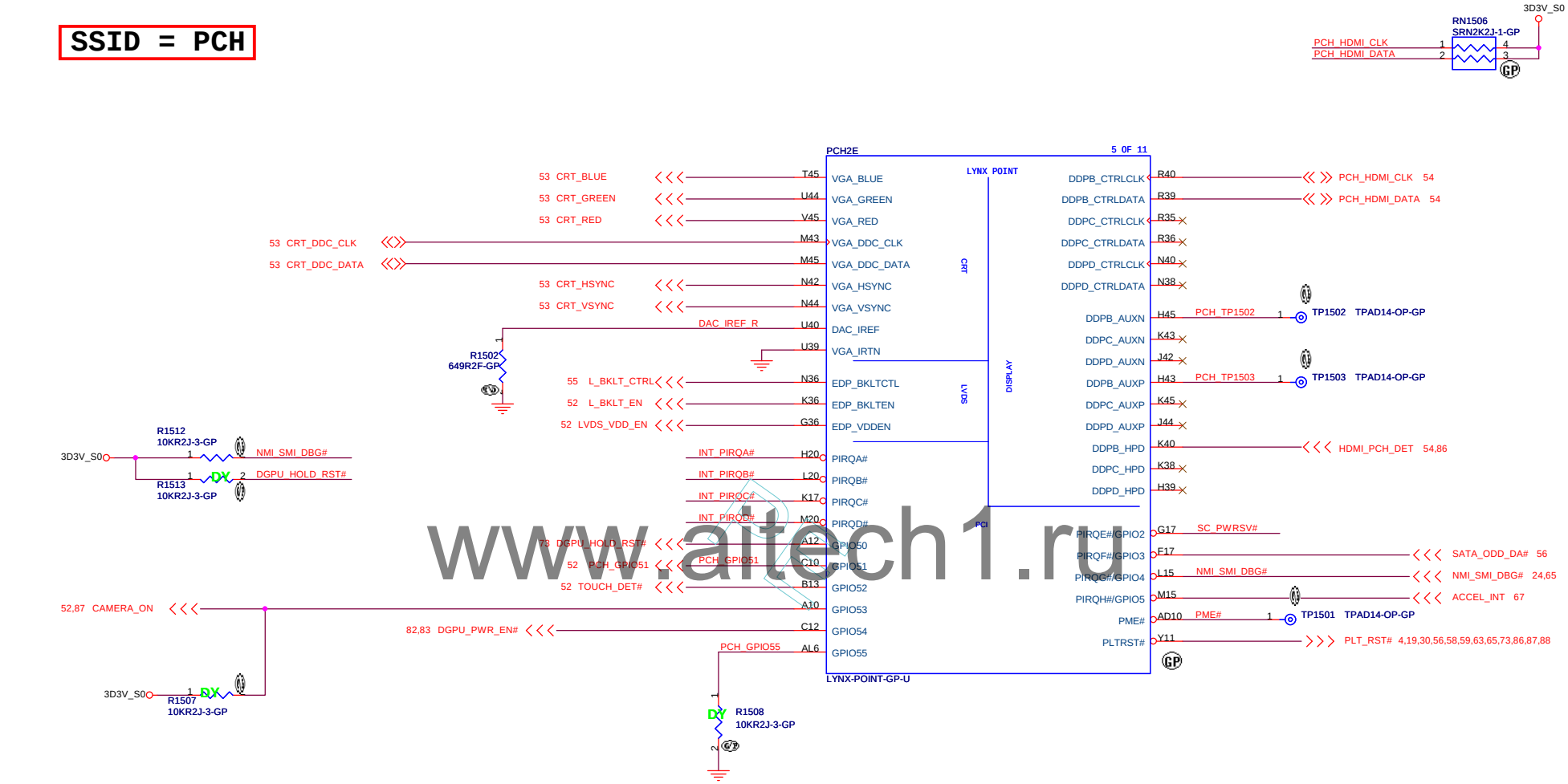
SSID = PCH



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BOOT BIOS Strap		
GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

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Title: PCH (PCI/CRT/DDI)

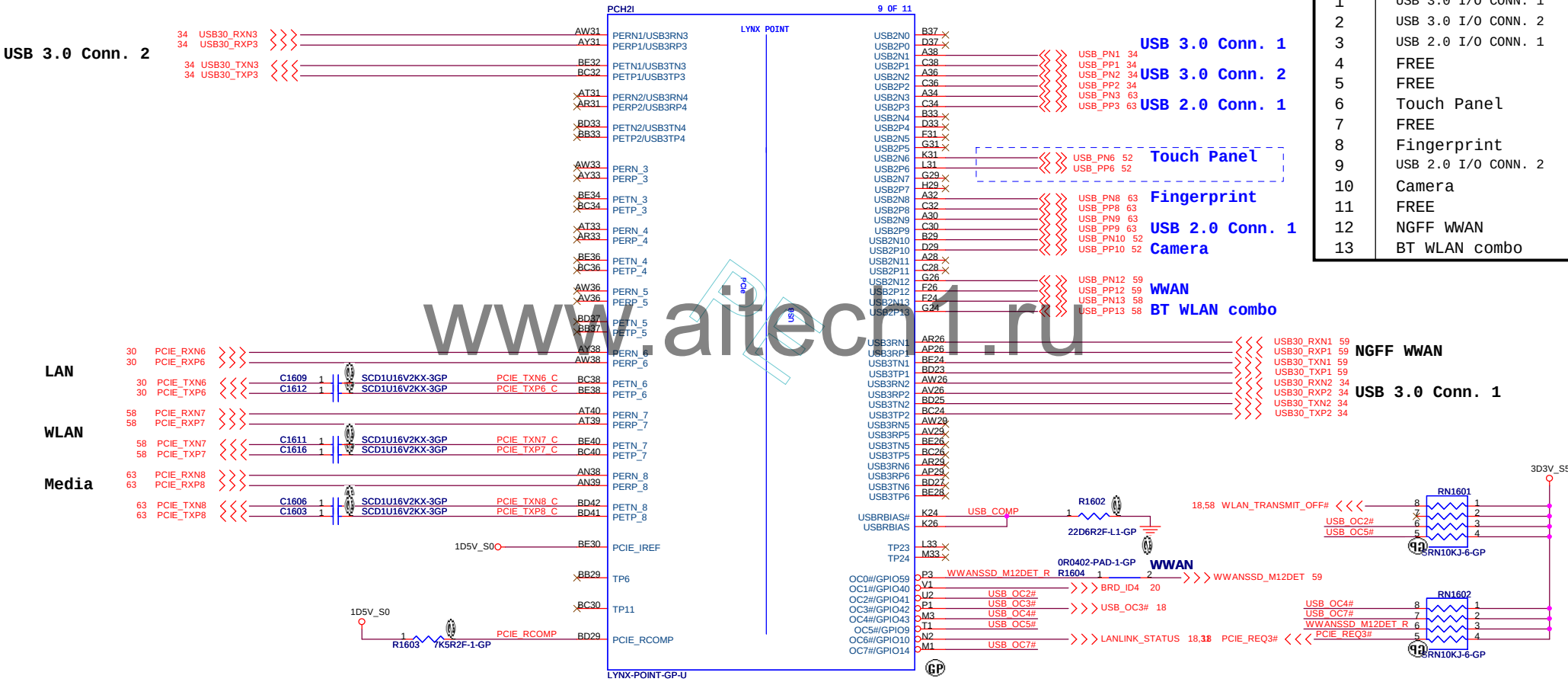
Size: A3 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

Date: Monday, August 12, 2013 | Sheet 15 of 103

SSID = PCH

USB2.0 Table

USB	
Pair	Device
0	FREE
1	USB 3.0 I/O CONN. 1
2	USB 3.0 I/O CONN. 2
3	USB 2.0 I/O CONN. 1
4	FREE
5	FREE
6	Touch Panel
7	FREE
8	Fingerprint
9	USB 2.0 I/O CONN. 2
10	Camera
11	FREE
12	NGFF WWAN
13	BT WLAN combo



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Title: PCH (PCIE/USB)

Size: A3 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

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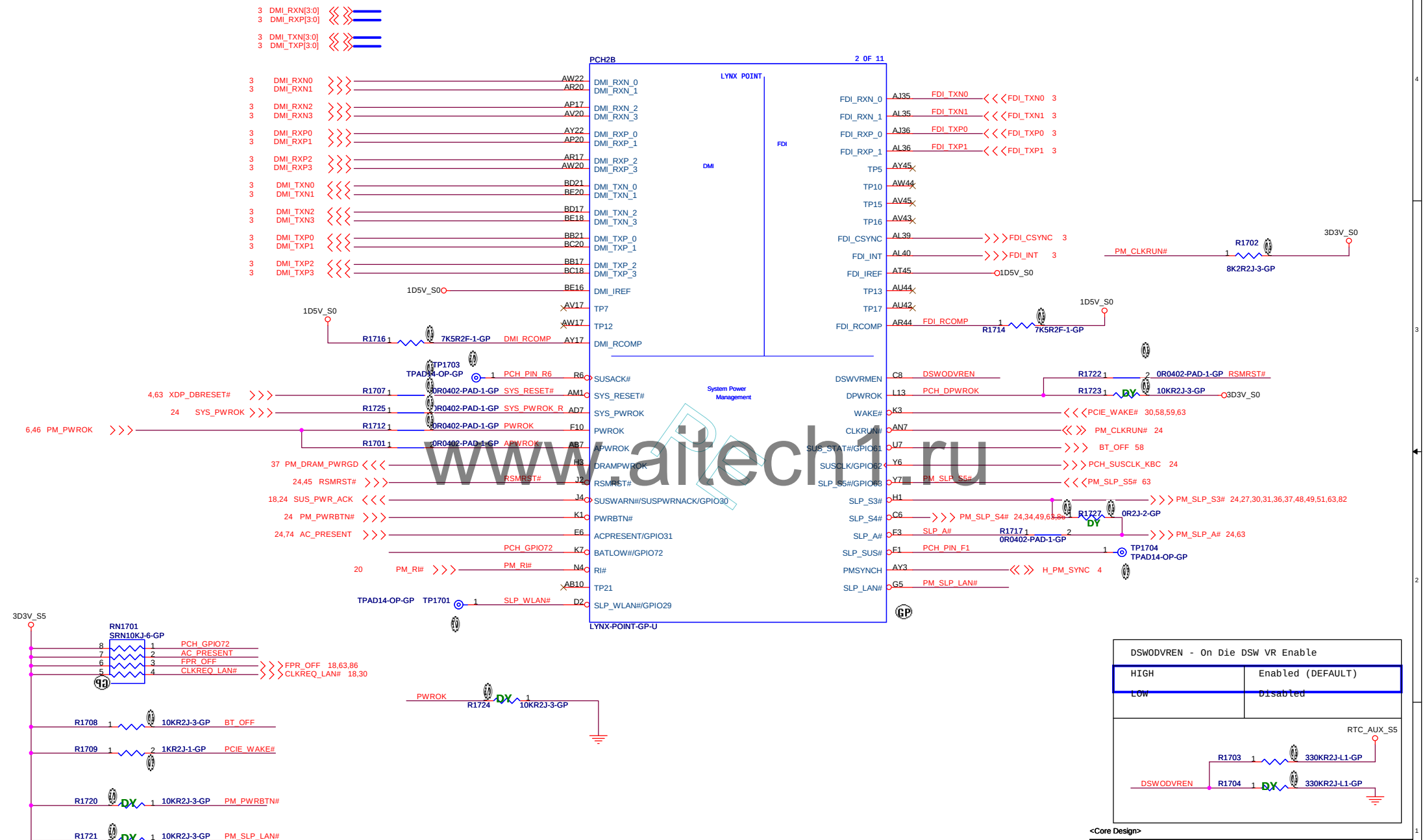
SSID = PCH



DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

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Title: PCH (DMI/FDI/PM)

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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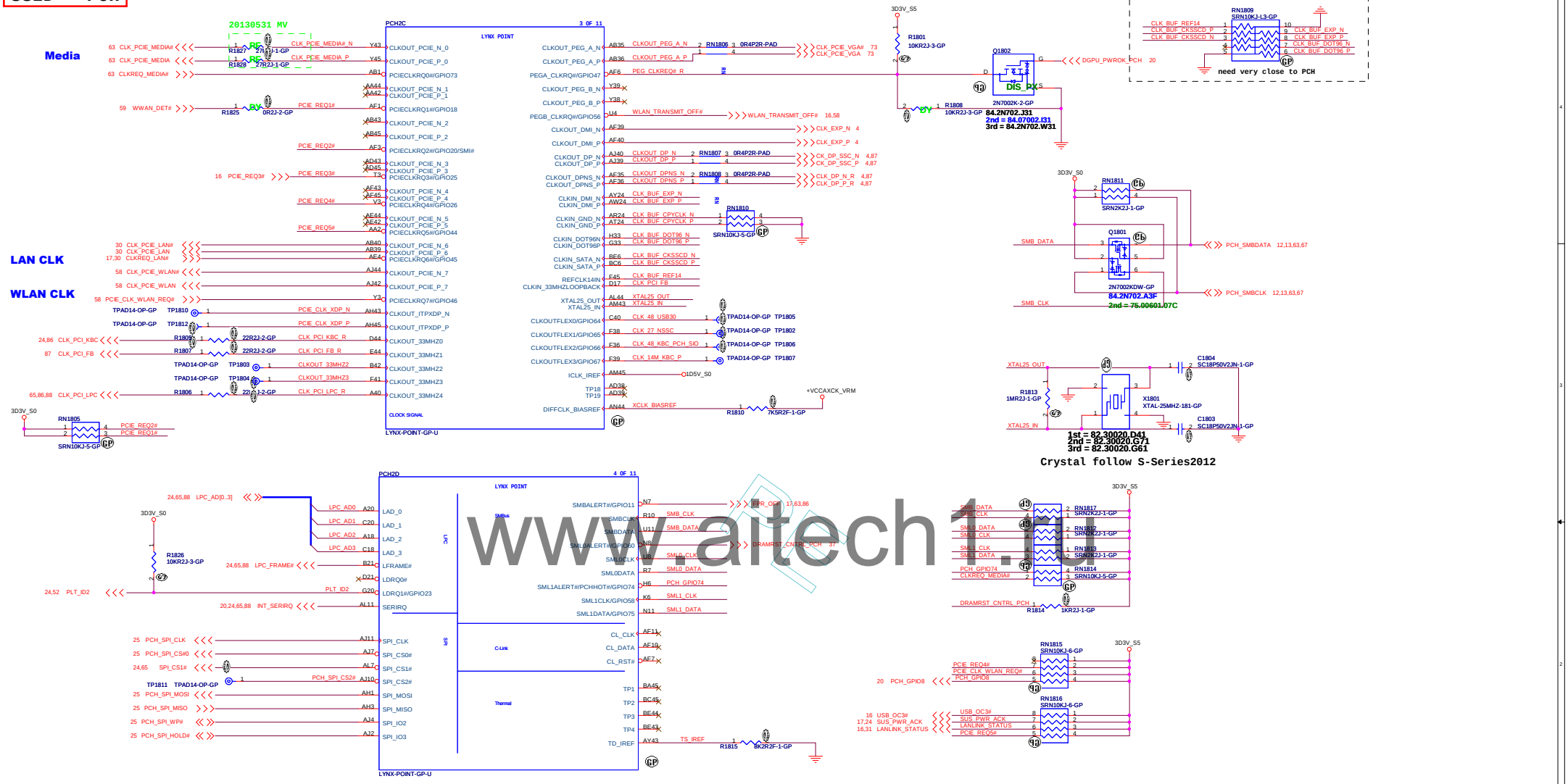
SSID = PCH

20130531 MV

Media

LAN CLK

WLAN CLK



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Title: PCH (PCI-E/SMBUS/CLOCK/CL)

Size: A2 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

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SSID = PCH

Close to PCH

INTVRMEN- Integrated SUS 1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs

Flash Descriptor Security Overide	
HDA_SDOUT	Low = Default High = Enable

No Reboot Strap	
HDA_SPKR	Low = Default High = No Reboot

HDA_SYNC:
HDA_SYNC signal also serves as a strap for selecting VRM voltage to the PCH. The strap
is sampled on the rising edge of RSMRST# signal. Due to potential leakage on the codec (path to GND), the strap may not be able to achieve the Vihmin at PCH input. Therefore, platform may need to isolate this signal from the codec during the strap phase.

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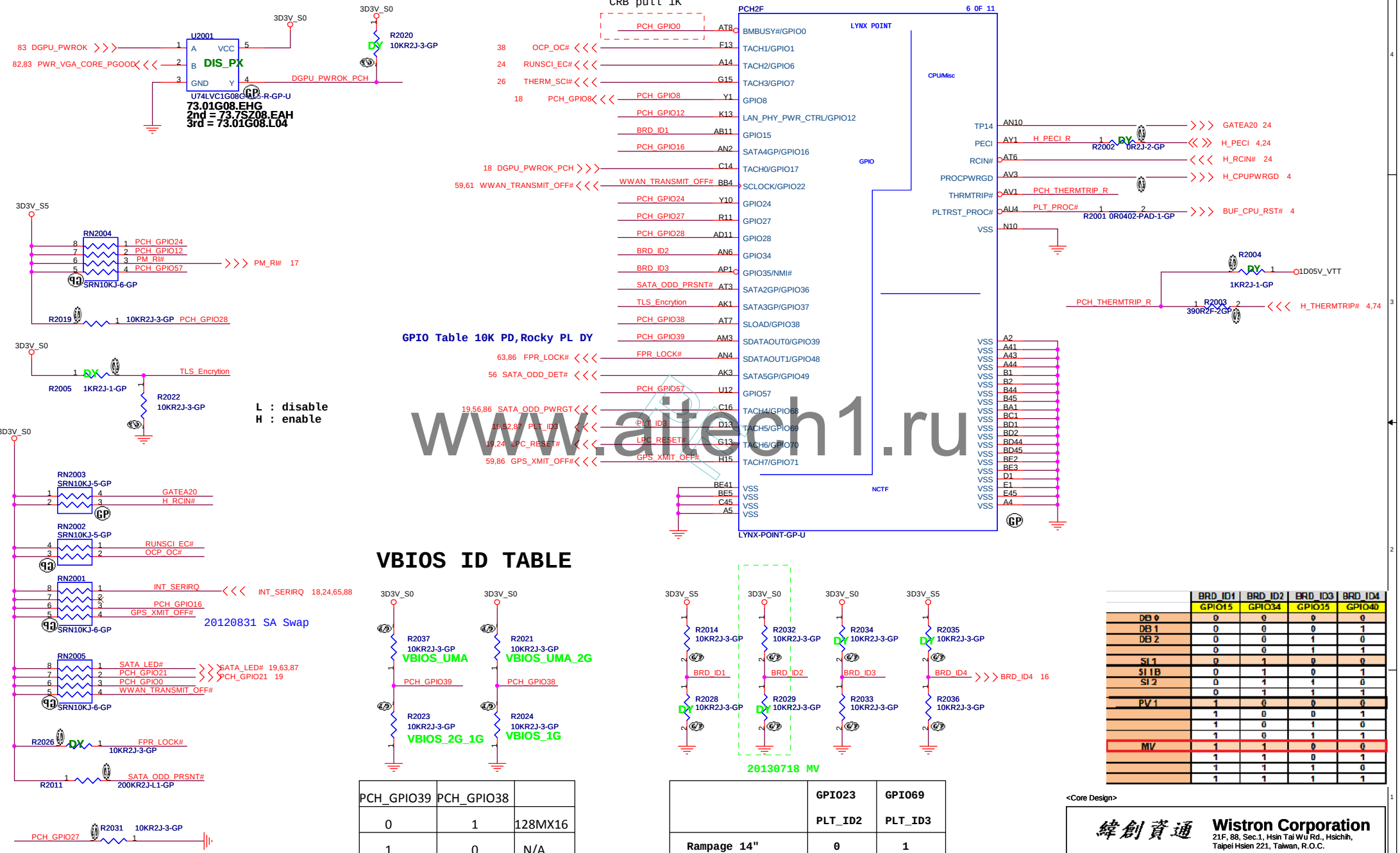
Title: PCH (RTC/SATA/IHDA/JTAG)
Size: A3 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1
Date: Monday, August 12, 2013 | Sheet 19 of 103

SSID = PCH



www.aiteh1.ru

PCH_GPIO39	PCH_GPIO38	
0	1	128MX16
1	0	N/A
1	1	UMA
0	0	64MX16

	GPIO23 PLT_ID2	GPIO69 PLT_ID3
Rampage 14"	0	1
Renegade 15"	1	0
Ricochet 17"	1	1

	BRD_ID1 GPIO15	BRD_ID2 GPIO34	BRD_ID3 GPIO35	BRD_ID4 GPIO40
DB 0	0	0	0	0
DB 1	0	0	0	1
DB 2	0	0	1	0
	0	0	1	1
SI 1	0	1	0	0
SI 1B	0	1	0	1
SI 2	0	1	1	0
	0	1	1	1
PV 1	1	0	0	0
	1	0	0	1
	1	0	1	0
	1	0	1	1
MV	1	1	0	0
	1	1	0	1
	1	1	1	0
	1	1	1	1

<Core Design>

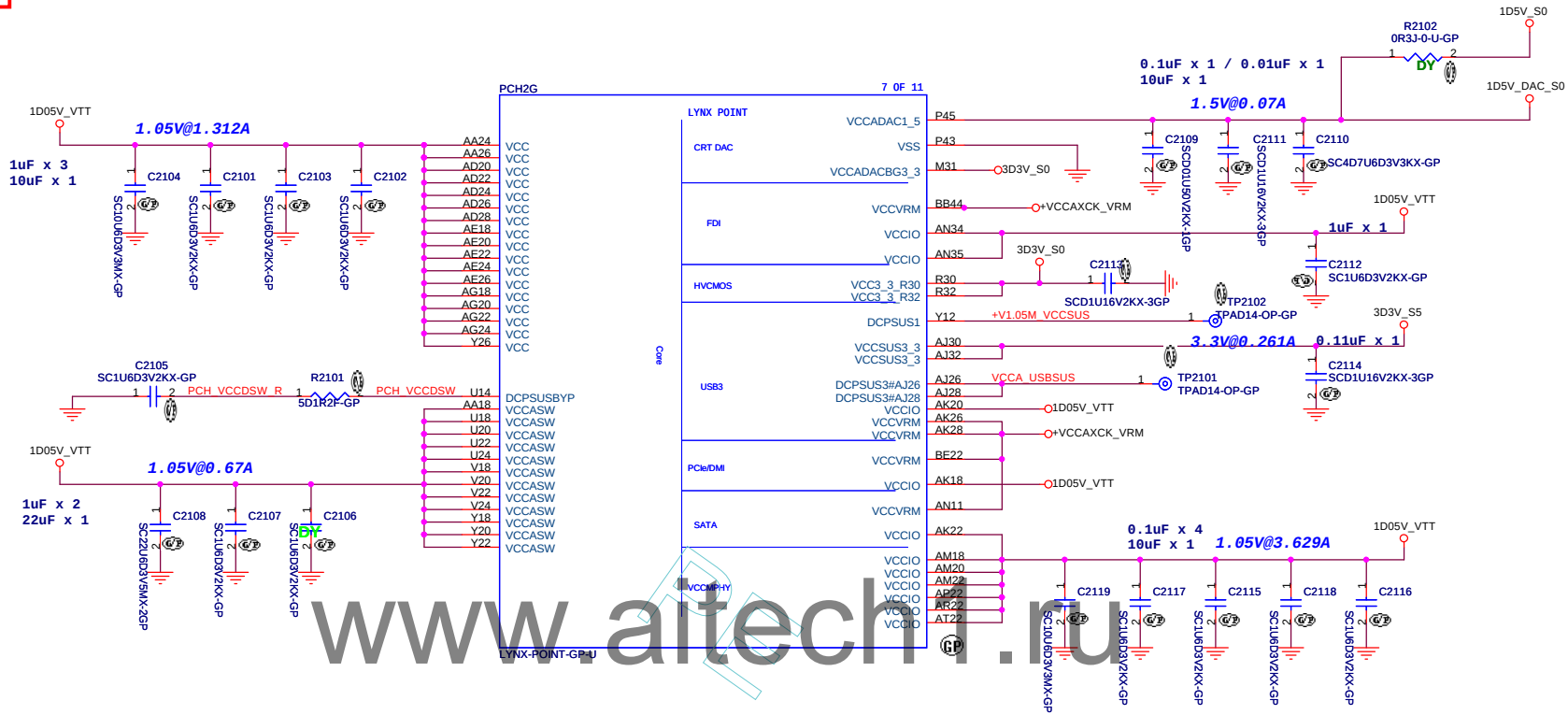
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

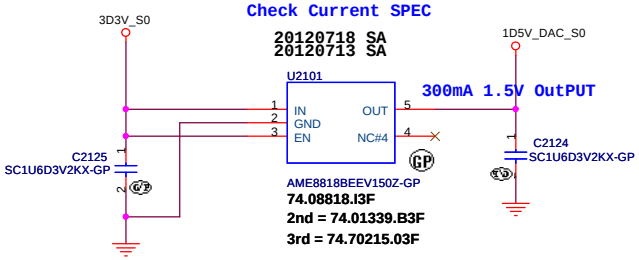
Title: PCH (GPIO/CPU)

Size: A3 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

Date: Monday, August 12, 2013 | Sheet 20 of 103

SSID = PCH





www.altech.ru

<Core Design>

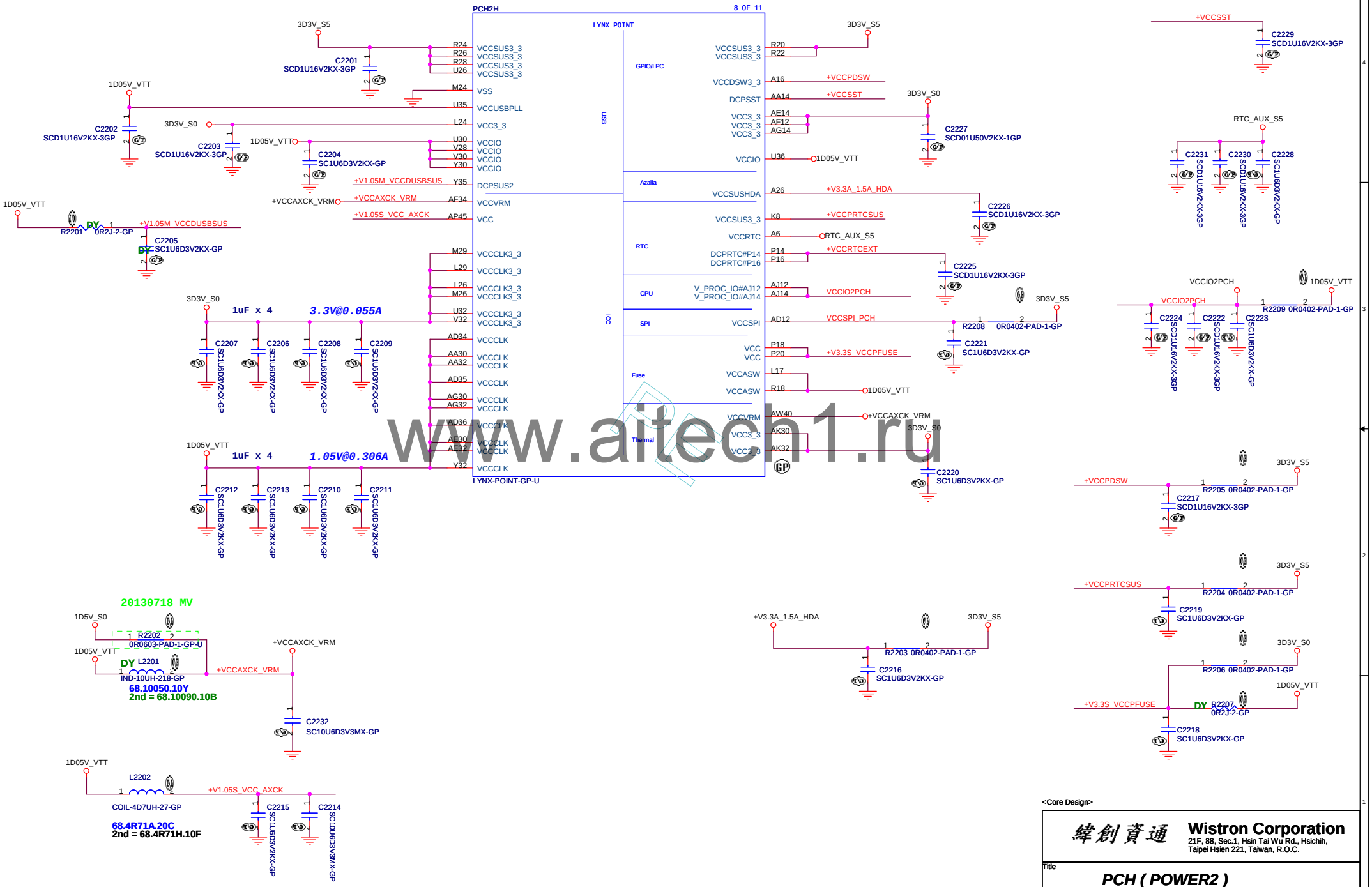
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PCH (POWER1)***

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

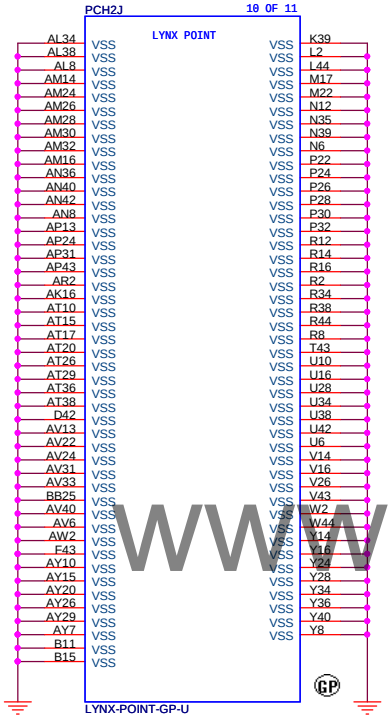
Date: Wednesday, July 24, 2013 Sheet 21 of 103

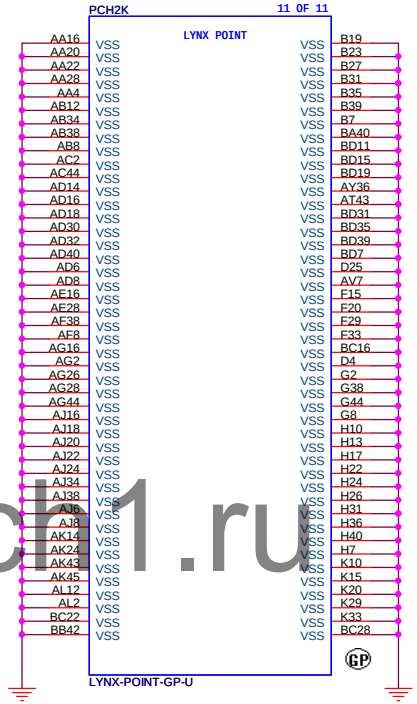
SSID = PCH



www.aitech1.ru

SSID = PCH





www.aitech1.ru

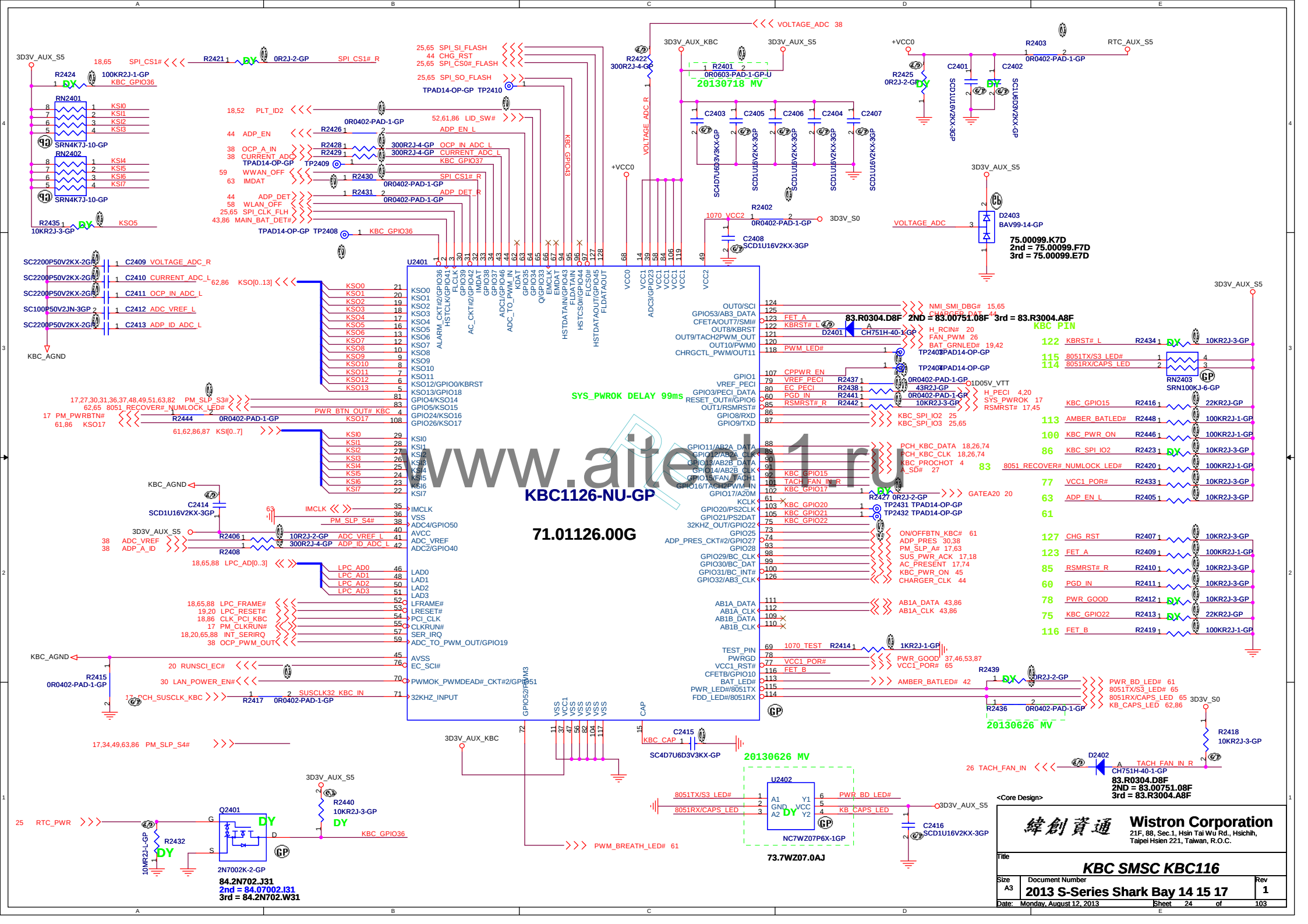
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PCH(VSS)***

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

Date: Wednesday, July 03, 2013 Sheet 23 of 103


KBC1126-NU-GP
71.01126.00G
SYS_PWROK DELAY 99ms
83.R0304.D8F 2ND = 83.00751.08F 3rd = 83.R3004.A8F
20130718 MV
20130626 MV
75.00099.K7D
2nd = 75.00099.F7D
3rd = 75.00099.E7D
84.2N702.J31
2nd = 84.07002.I31
3rd = 84.2N702.W31
73.7WZ07.0AJ
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC SMSC KBC116
2013 S-Series Shark Bay 14 15 17
Monday, August 12, 2013
www.alteh1.ru

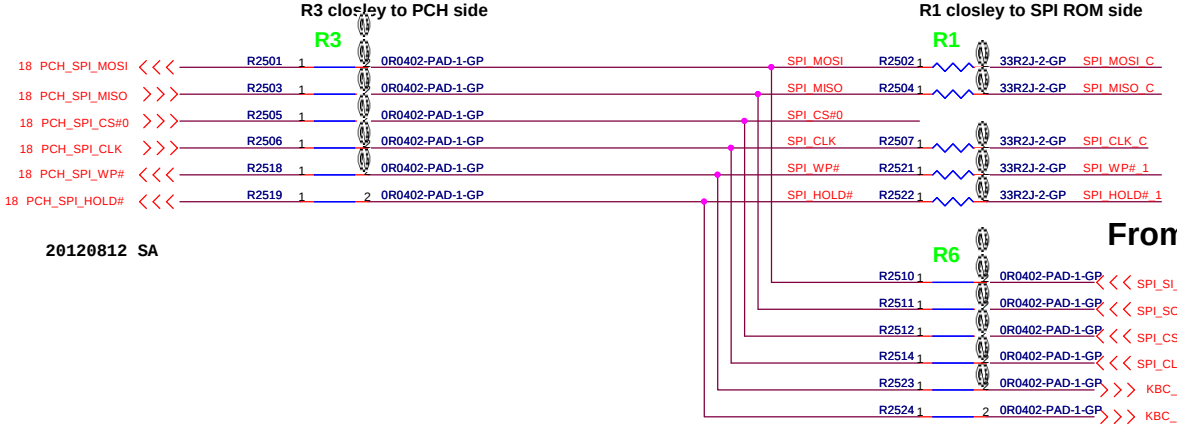
SPI FLASH ROM (8M byte) for PCH

To PCH

From BIOS

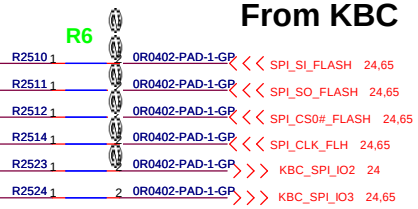
R3 closley to PCH side

R1 closley to SPI ROM side



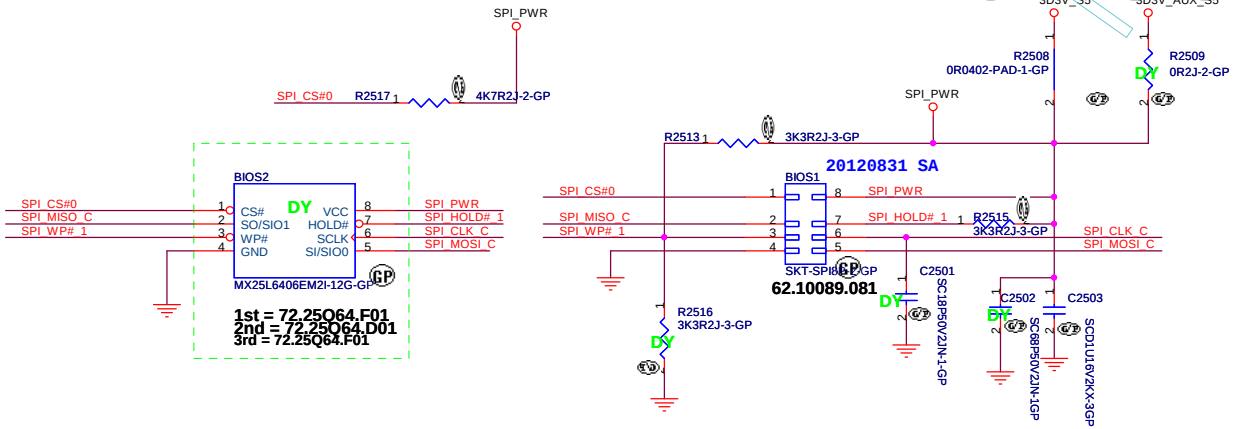
20120812 SA

From KBC



SPI_CLK — SPI_CLK 87 — To RF CAP

SYSTEM SPI ROM Socket

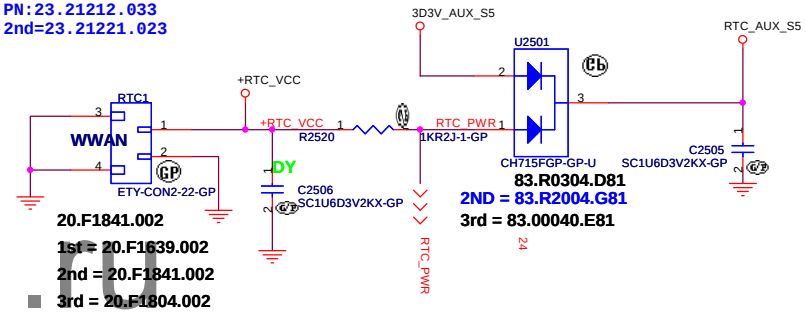


NOTE: SPI signal use GND reference

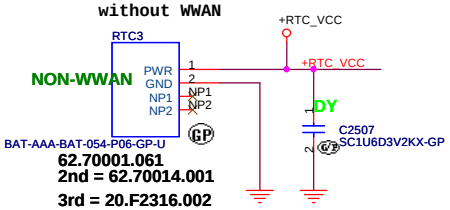
Quad IO Winbond 8M:72.25Q64.K01 (W25Q64FVSSIQ)
MXIC : 72.25647.00A (MX25L6473EM2I)
Micon: 72.25Q64.G01 (N25Q064A13ESEC0F)

RTC Battery

RTC Battery+Cable
PN:23.21212.033
2nd=23.21221.023



without WWAN



RTC Battery PN:23.22065.001
23.22063.001
23.20068.001

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

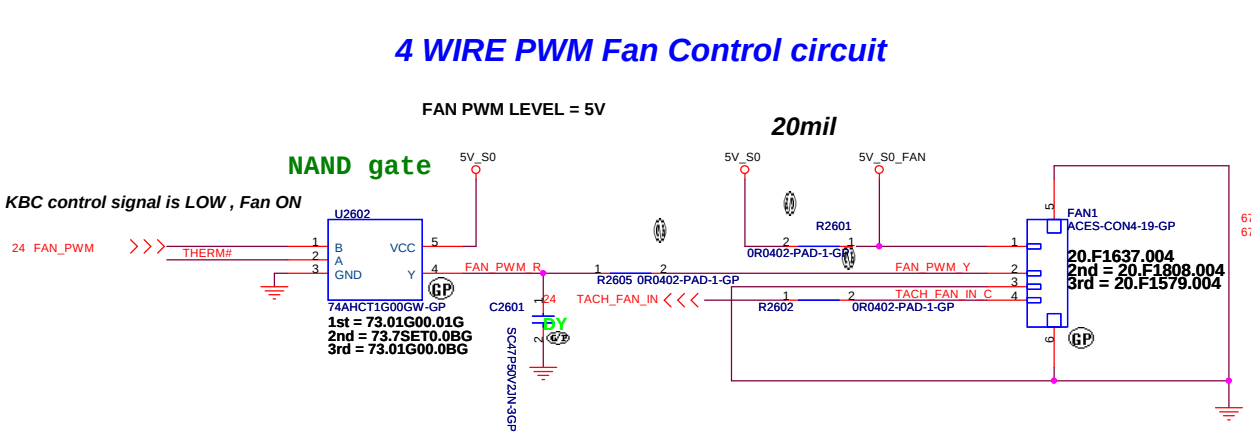
Title: Flash(KBC+PCH)/RTC

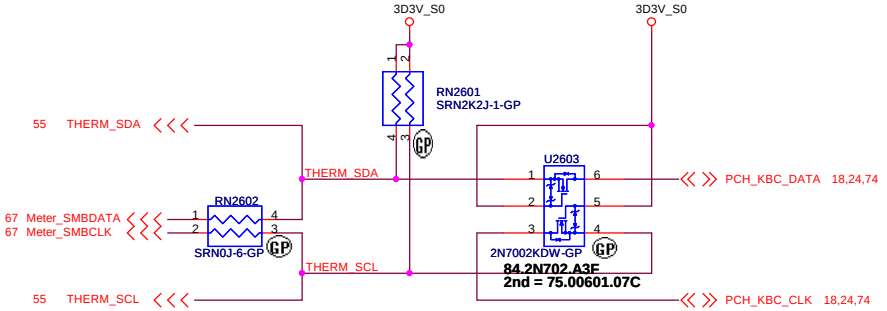
Size: A3 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

Date: Monday, August 12, 2013 | Sheet 25 of 103

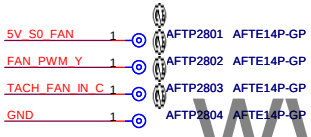
Thermal Sensor,FAN

4 WIRE PWM Fan Control circuit

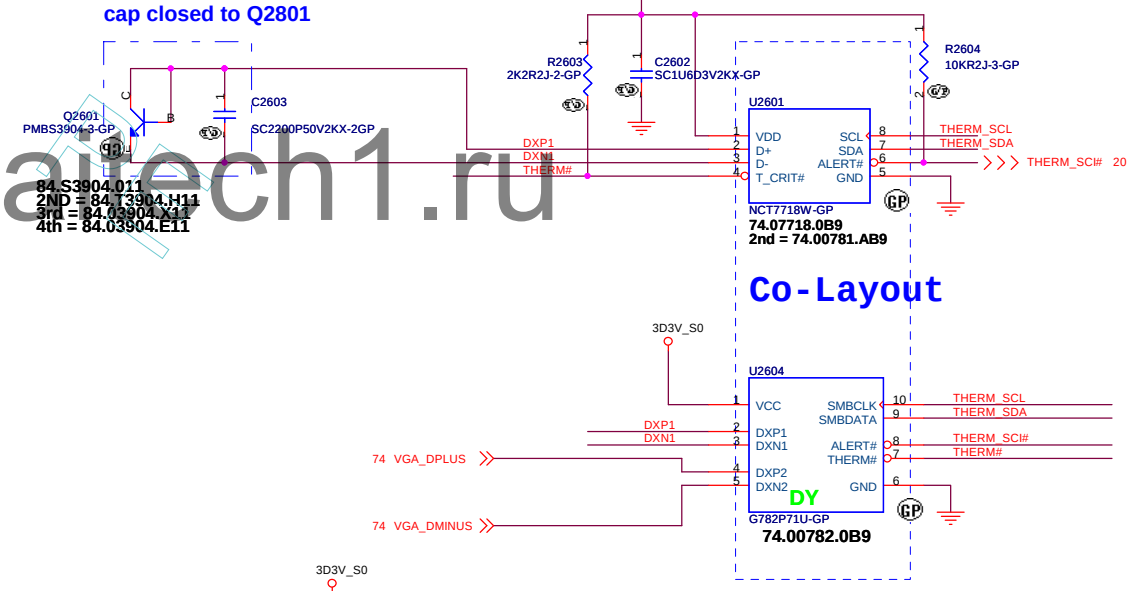




A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L



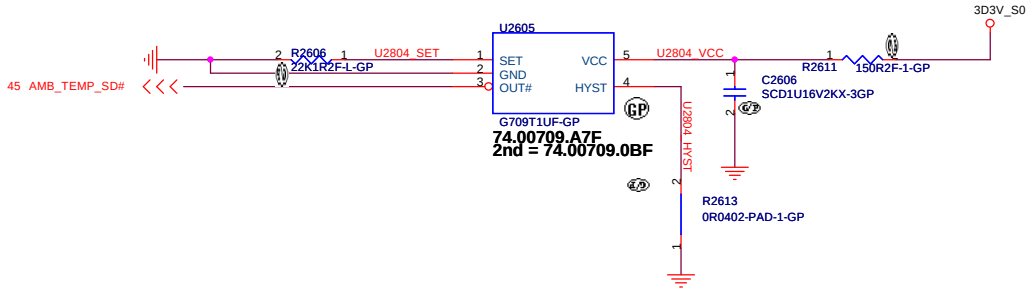
Thermal IC Control circuit



Co-Layout

T8 H/W Shutdown Control circuit

Degree	Rset
95	25.5K
90	22.1K
85	18.7K



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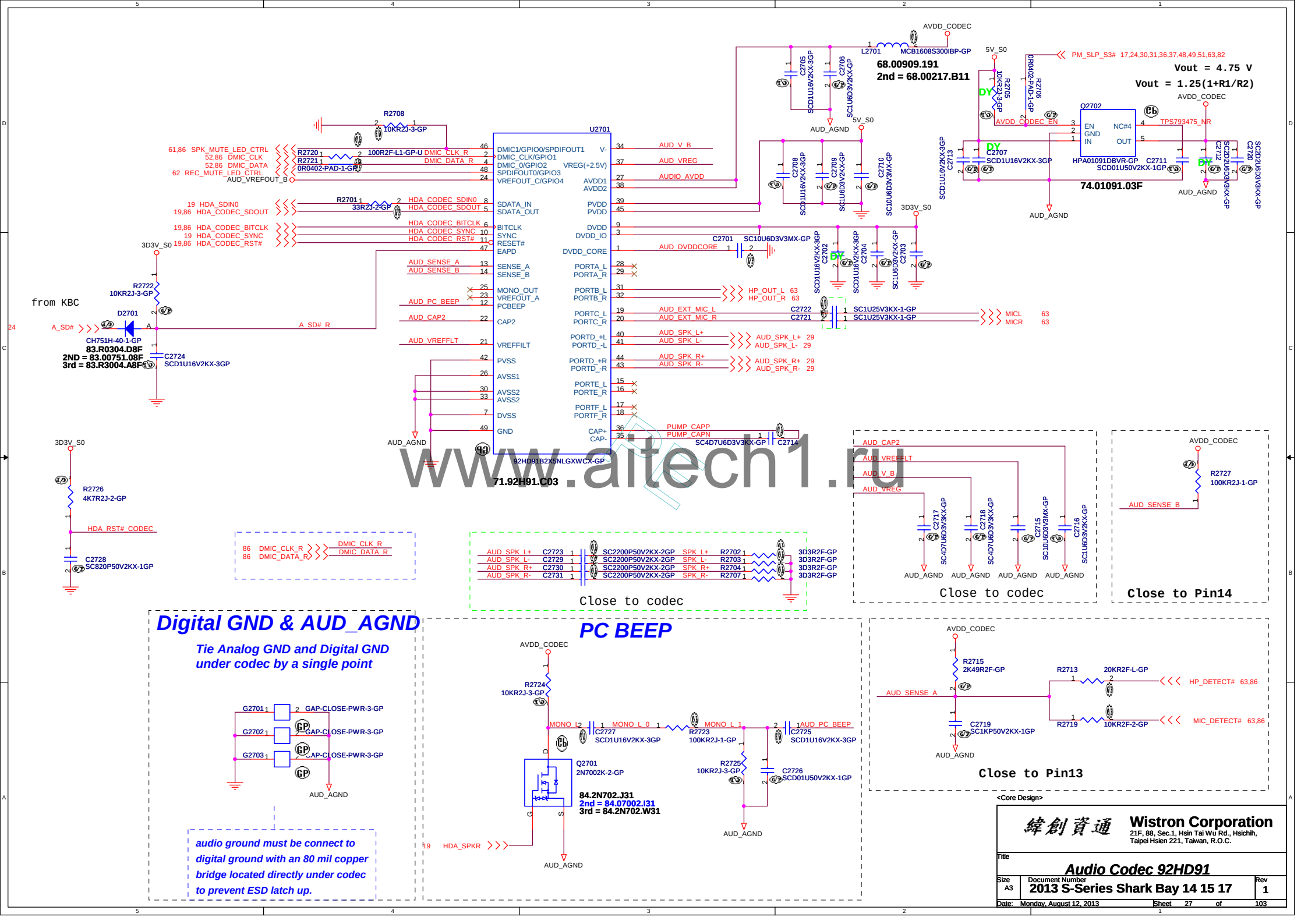
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal G781/Fan control

Size: A3 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

Date: Monday, August 12, 2013 | Sheet 26 of 103



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec 92HD91

Size: A3 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

Date: Monday, August 12, 2013 | Sheet 27 of 103

www.aitech1.ru

<Variant Name>

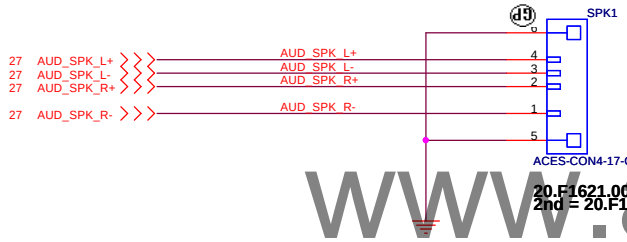
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

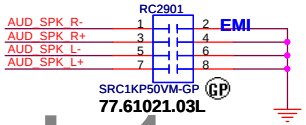
Title: ***AUDIO AMP(Reserved)***

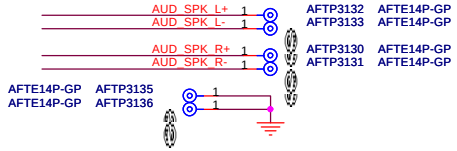
Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

Date: Wednesday, July 03, 2013 Sheet 28 of 103

Speaker Connector







www.aitech1.ru

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MIC/SPEAKER/AUDIO JACK

Size: A3 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

Date: Monday, August 12, 2013 | Sheet 29 of 103

LAN RJ45

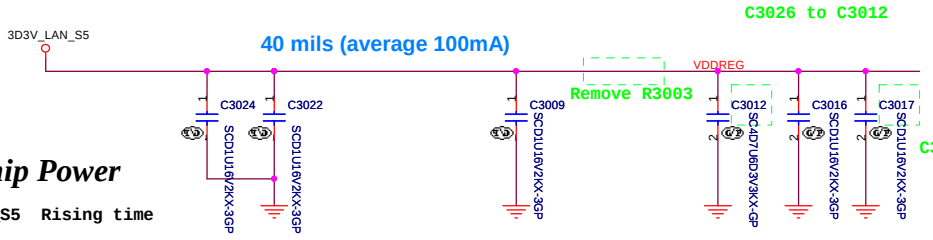
USE EFuse No ASF

DEL

LAN CHIP-RTL8151GH

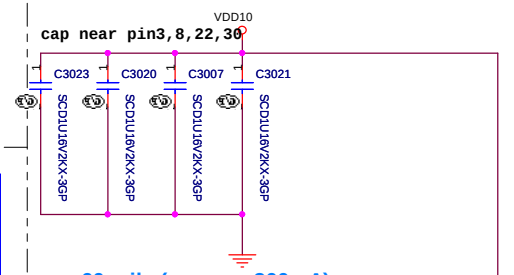
LanChip Power

+3.3V_LAN_S5 Rising time (10%~90%)
Spec >1mS and <100mS



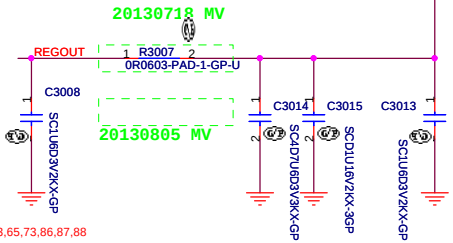
cap near pin11,32 <200mils

Regout power plane(1D05V)

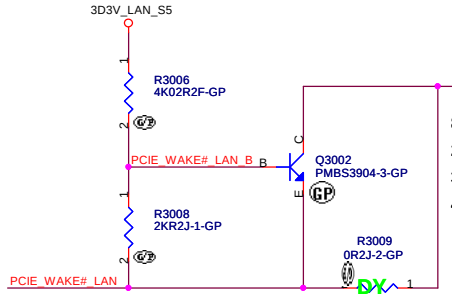


60 mils (average 300mA)

20130718 MV

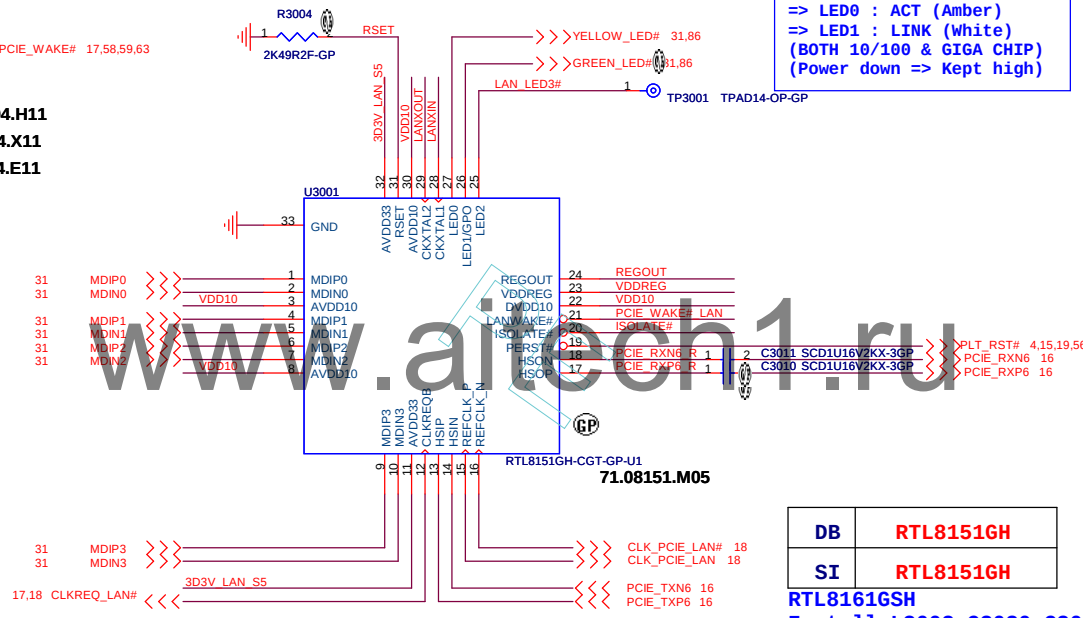


Put 4D7U L + 4D7U cap near pin24 <200mils
(2nd = 78.22610.81L)



84.S3904.011
2nd = 84.T3904.H11
3rd = 84.03904.X11
4th = 84.03904.E11

EEPROM LED OPTION USE '00'
=> LED0 : ACT (Amber)
=> LED1 : LINK (White)
(BOTH 10/100 & GIGA CHIP)
(Power down => Kept high)



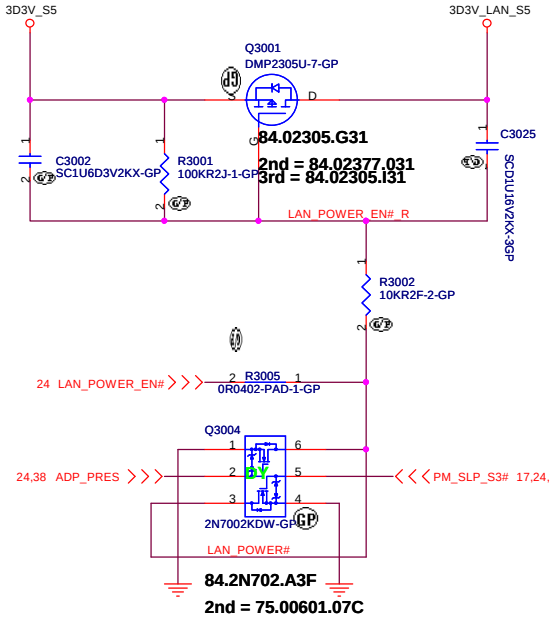
71.08151.M05

DB	RTL8151GH
SI	RTL8151GH

RTL8161GSH
Install:L3003 C3030 C3031 C3026 C3001
DY:R3007

Lan Power Inductance Spec
(1) IDC >= 600mA
(2) Tolerance < 20%
(3) RDC <= 0.8ohms(Max)
(4) Efficiency >= 80%

3D3V_LAN_S5 rise time controlled between 0.5mS and 100mS.

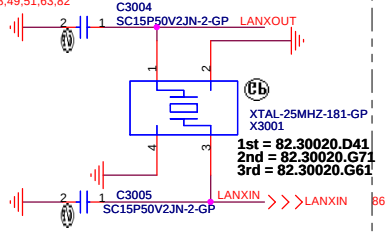


84.02305.G31
2nd = 84.02377.031
3rd = 84.02305.I31

84.2N702.A3F
2nd = 75.00601.07C

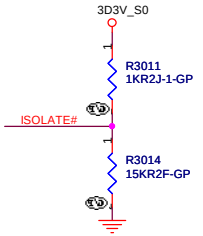
Using Efuse
Without ASF

25MHz Crystal



1st = 82.30020.D41
2nd = 82.30020.G71
3rd = 82.30020.G61

Isolate Strap Pin



Regout Switch

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Lan Realtek 8151GH

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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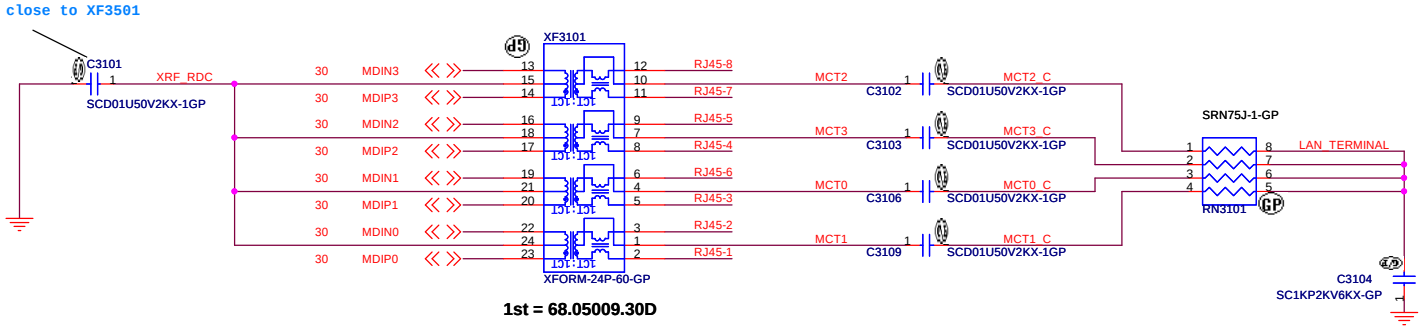
White LED for connectivity and Amber LED for activity located on RJ-45 connector



1st = 68.05009.30D
2nd = 68.89240.30D
3rd = 68.IH601.301

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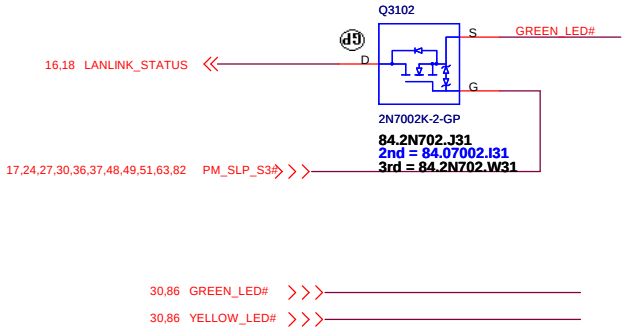
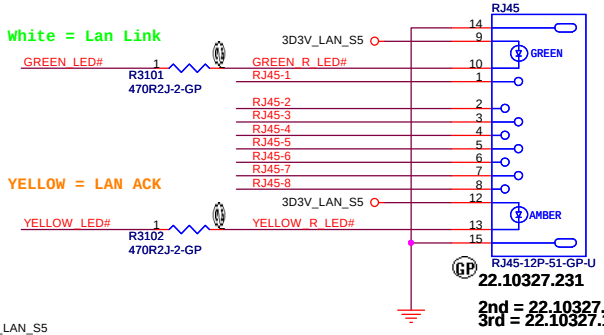
RJ45 Connector



84.2N702.J31
2nd = 84.07002.I31
3rd = 84.2N702.W31

wavelength : Orange 605mm need check

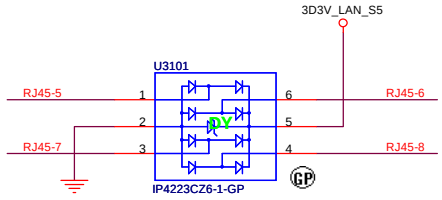


22.10327.231
2nd = 22.10327.151
3rd = 22.10327.171

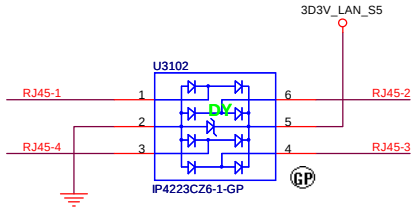
Green
10(+),9(-)

YELLOW
12(+),13(-)

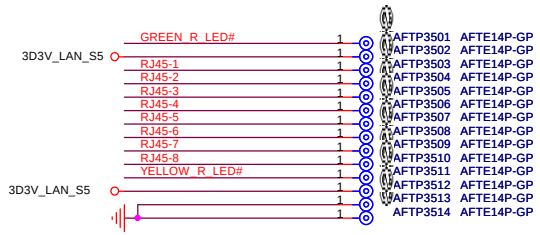
(1)route on bottom as differential pairs.
(2)Tx+/Tx- are pairs. Rx+/Rx- are pairs.
(3)No vias, No 90 degree bends.
(4)pairs must be equal lengths.
(5)6mil trace width,12mil separation.
(6)36mil between pairs and any other trace.
(7)Must not cross ground moat,
except RJ-45 moat.



75.04223.07C
2nd = 75.09904.07C
3rd = 75.02304.07C



75.04223.07C
2nd = 75.09904.07C
3rd = 75.02304.07C



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RJ45+Transformer

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Card Reader-JMB 709***

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

Date: Wednesday, July 03, 2013 Sheet 32 of 103

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<Variant Name>

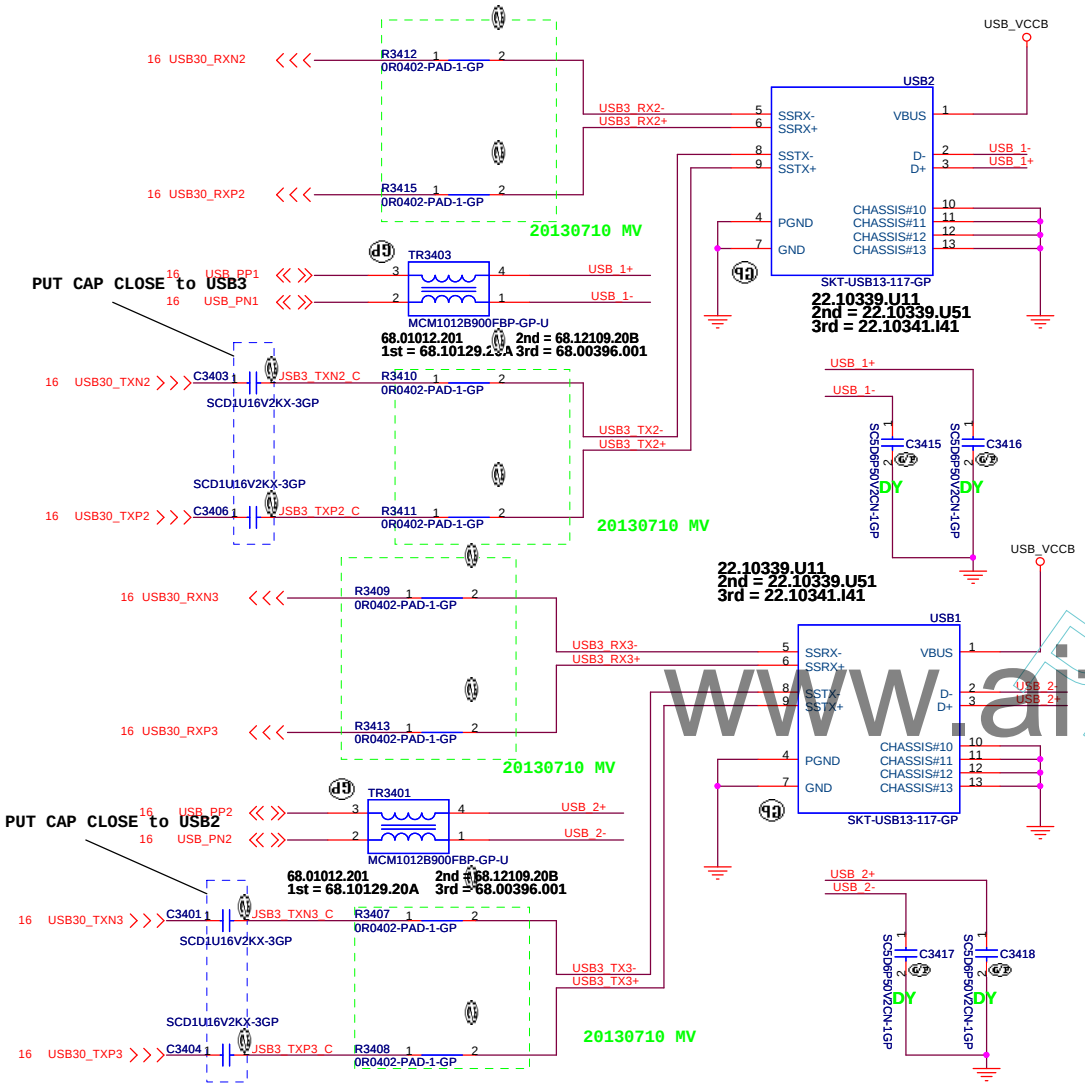
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
CARD Reader CONN

Size	Document Number	Rev
A3	**2013 S-Series Shark Bay 14 15 17**	1

Date: Wednesday, July 03, 2013 Sheet 33 of 103

Left Side USB 3.0 Connector



USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX-
6	StdA_SSRX+
7	GND
8	StdA_SSTX-
9	StdA_SSTX+

USB 3.0/2.0 Port Pairing

USB3.0	USB2.0
Port 1	Port 0
Port 2	Port 1
Port 3	Port 2
Port 4	Port 3
Port 5	Port 4
Port 6	Port 5

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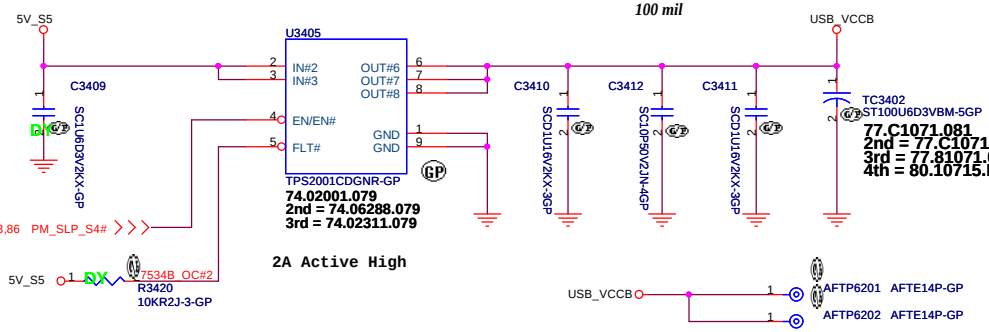
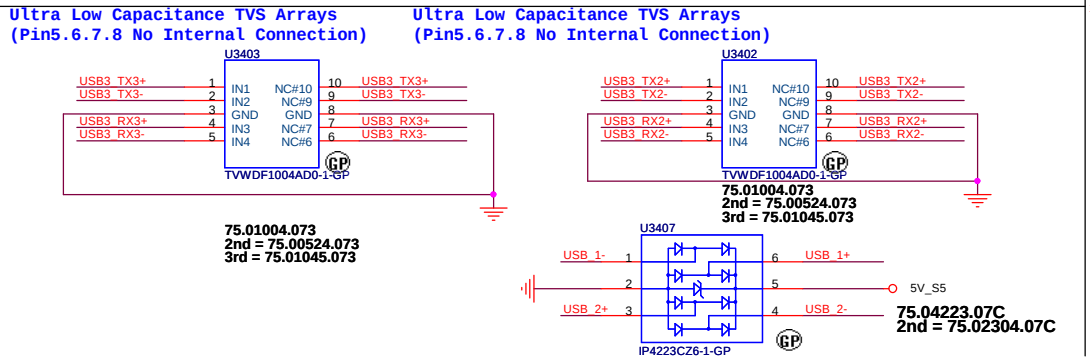
USB POWER





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Title: **USB 2.0/ 3.0 Port**

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Title: ***USB Charger***

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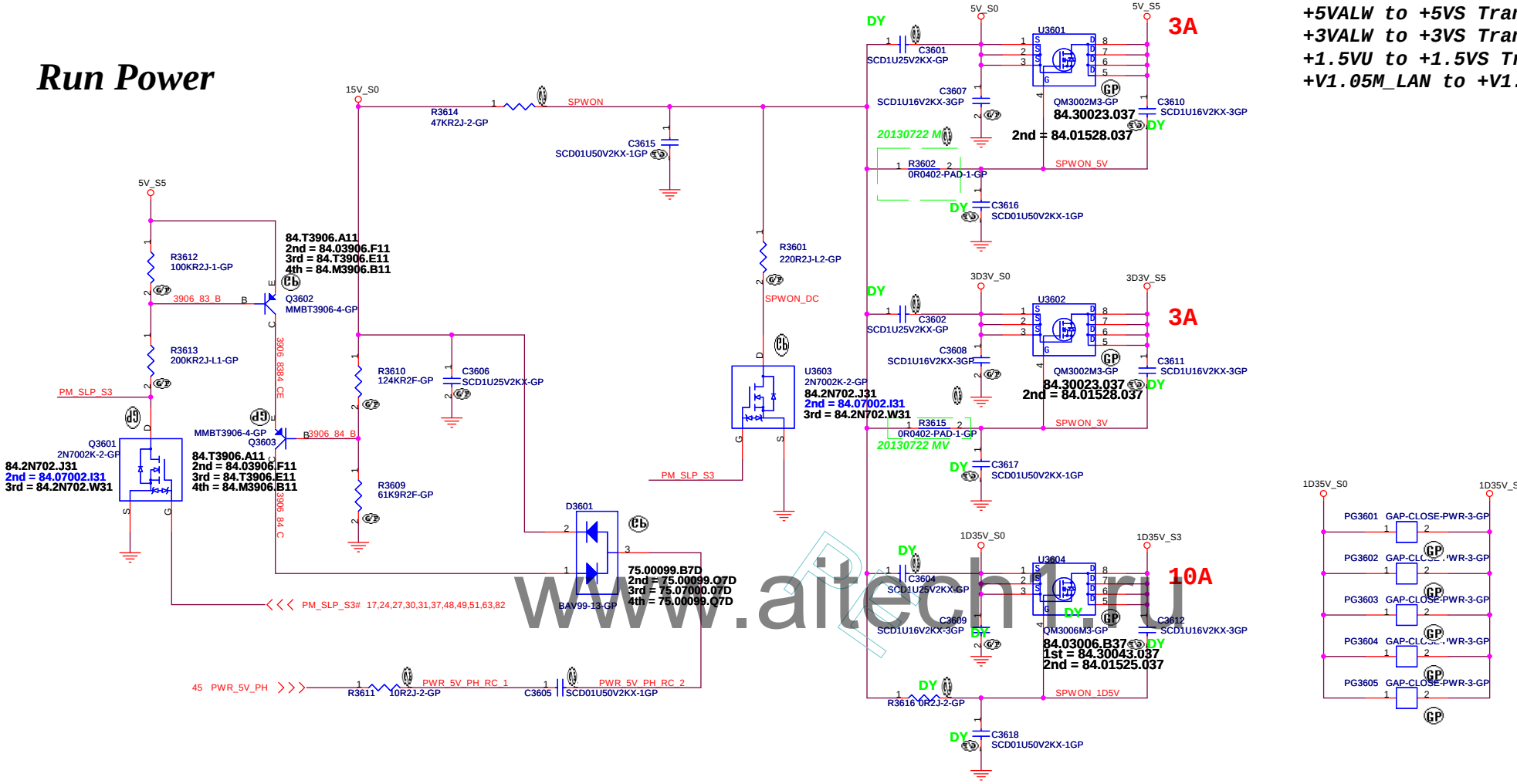
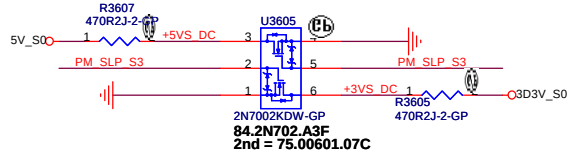
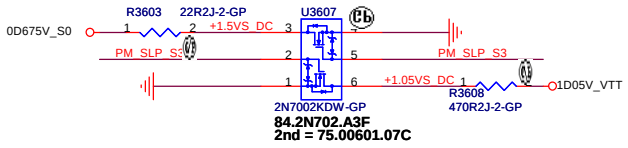
Run Power

+5VALW to +5VS Transfer
+3VALW to +3VS Transfer
+1.5VU to +1.5VS Transfer
+V1.05M_LAN to +V1.05S Transfer







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<Core Design>

緯創資通 Wistron Corporation
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Title: Power Plane Enable

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A3	2013 S-Series Shark Bay 14 15 17	1

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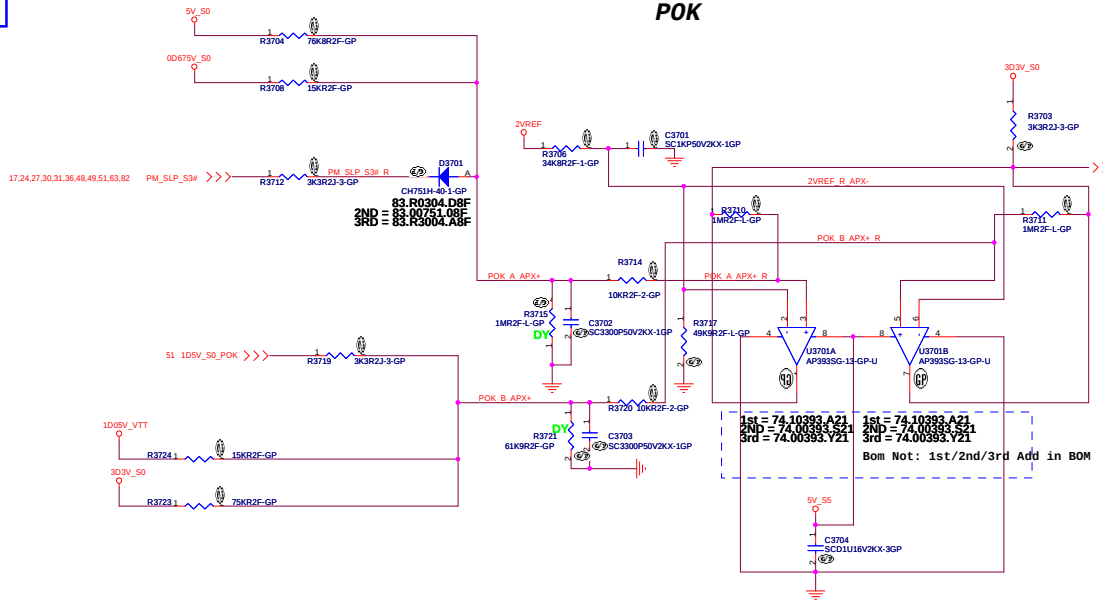
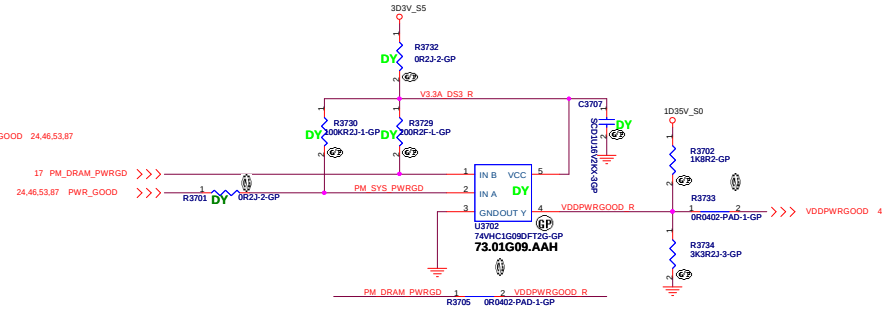
POK

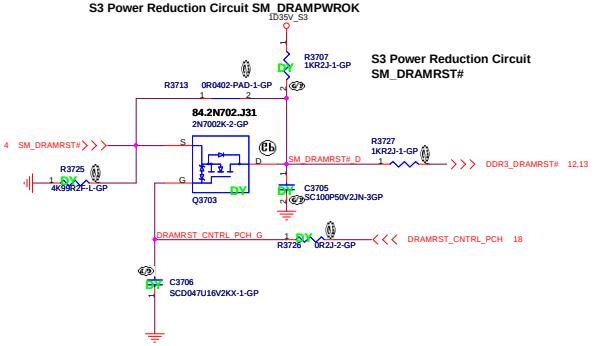
POK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



VREF circuit -M1 (Voltage Driver Network) & M3 (Driven by Processor) Implementation

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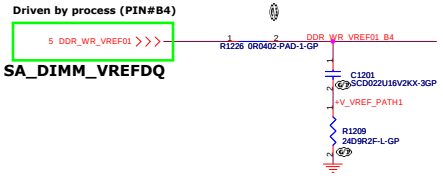

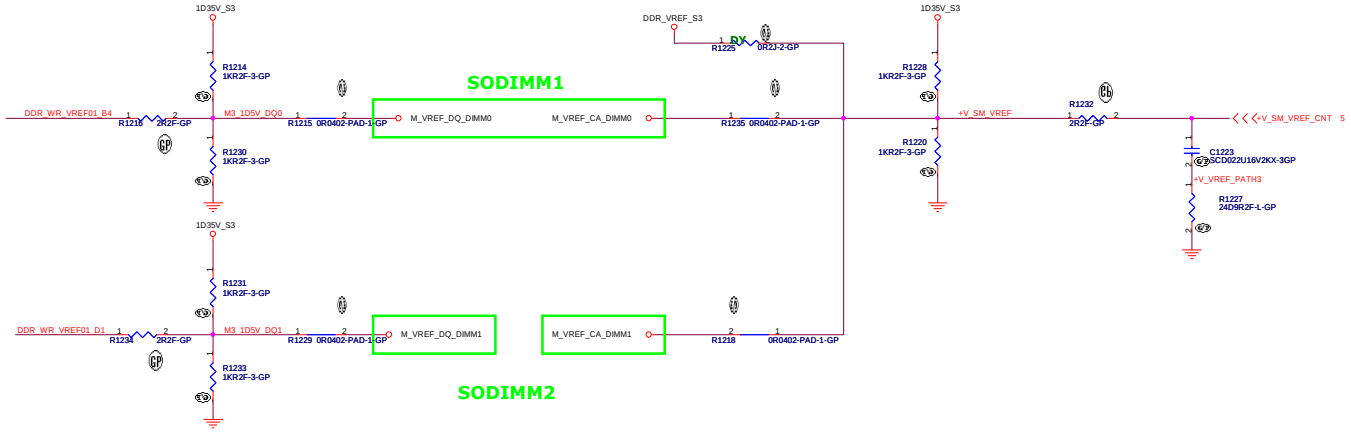

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Title: POK

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A2	2013 S-Series Shark Bay 14 15 17	1

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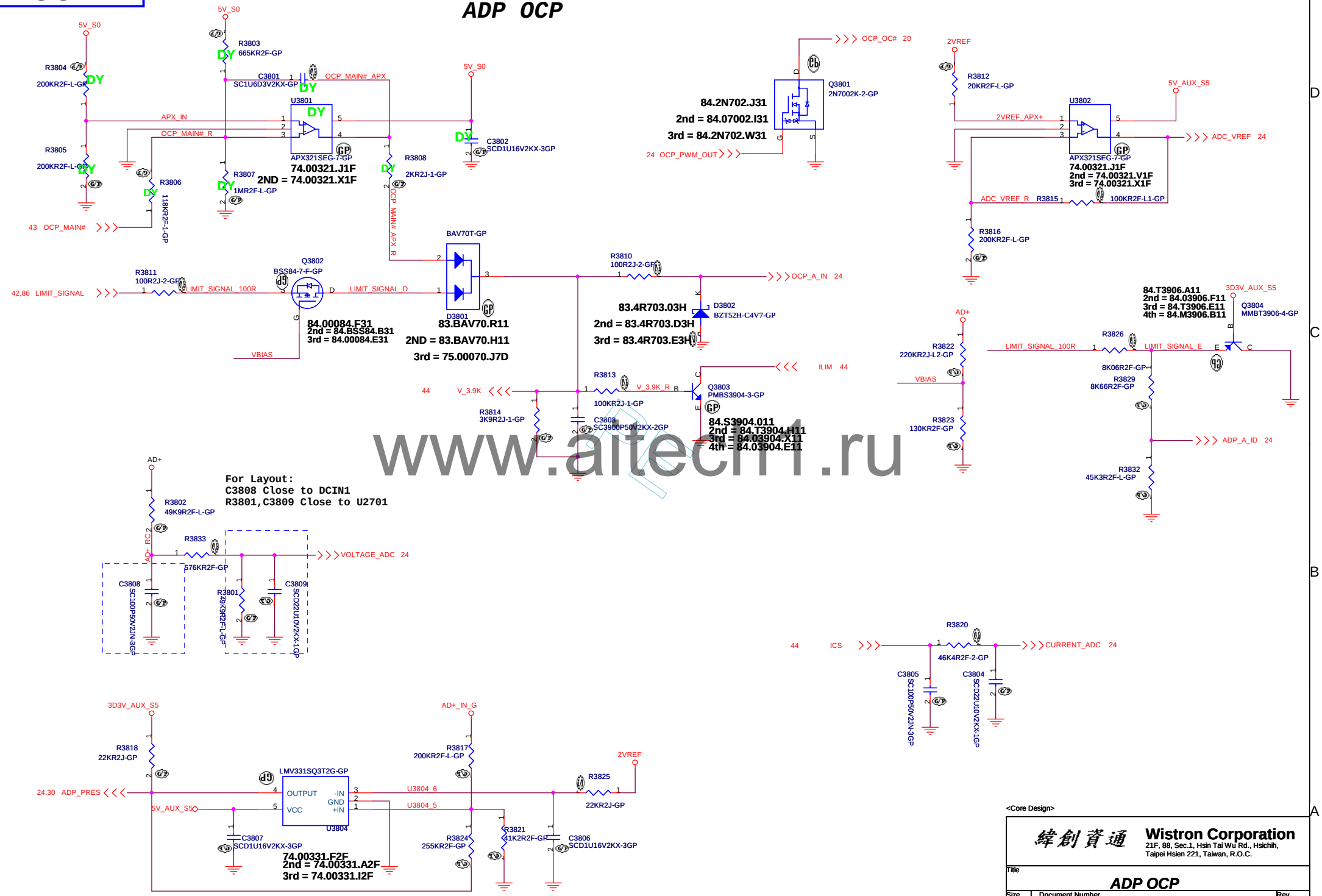
ADP OCP

ADP OCP



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Title: ADP OCP

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A3	2013 S-Series Shark Bay 14 15 17	1

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Title

1D05 M

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A3	**2013 S-Series Shark Bay 14 15 17**	1

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<Variant Name>

Title	<Title>	
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Title: *TPS51225_5V/3D3V*

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A2	2013 S-Series Shark Bay 14 15 17	1

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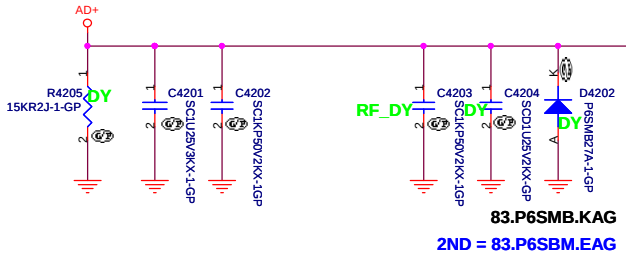
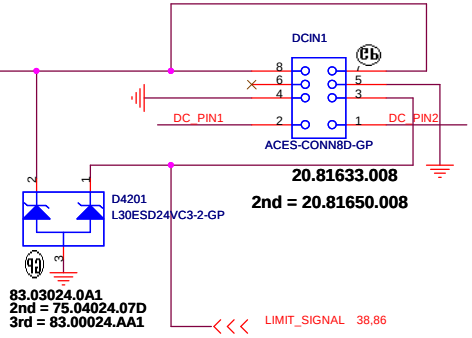
Adaptor in to generate DCBATOUT



83.P6SMB.KAG

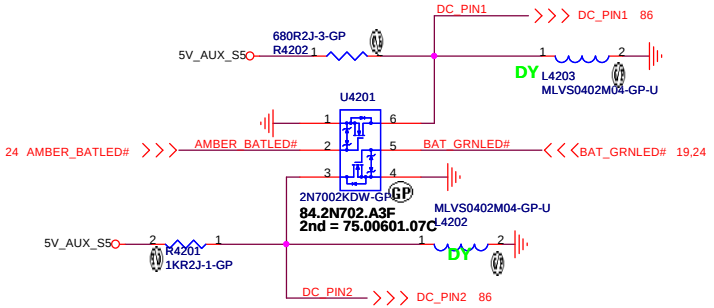
2ND = 83.P6SBM.EAG

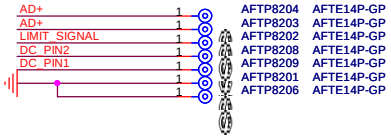


20.81633.008

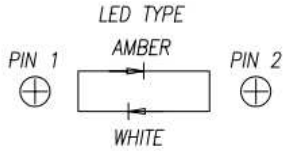
2nd = 20.81650.008

83.03024.0A1
2nd = 75.04024.07D
3rd = 83.00024.AA1





	KBC pin 120 BAT_GRNLED#	KBC pin 113 AMBER_BATLED#
Amber	High	Low
White	Low	High
LED OFF	Low	Low



NODE		COLOR
PIN1(+)	PIN2(−)	AMBER
PIN1(−)	PIN2(+)	WHITE

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Title: **DCIN JACK**

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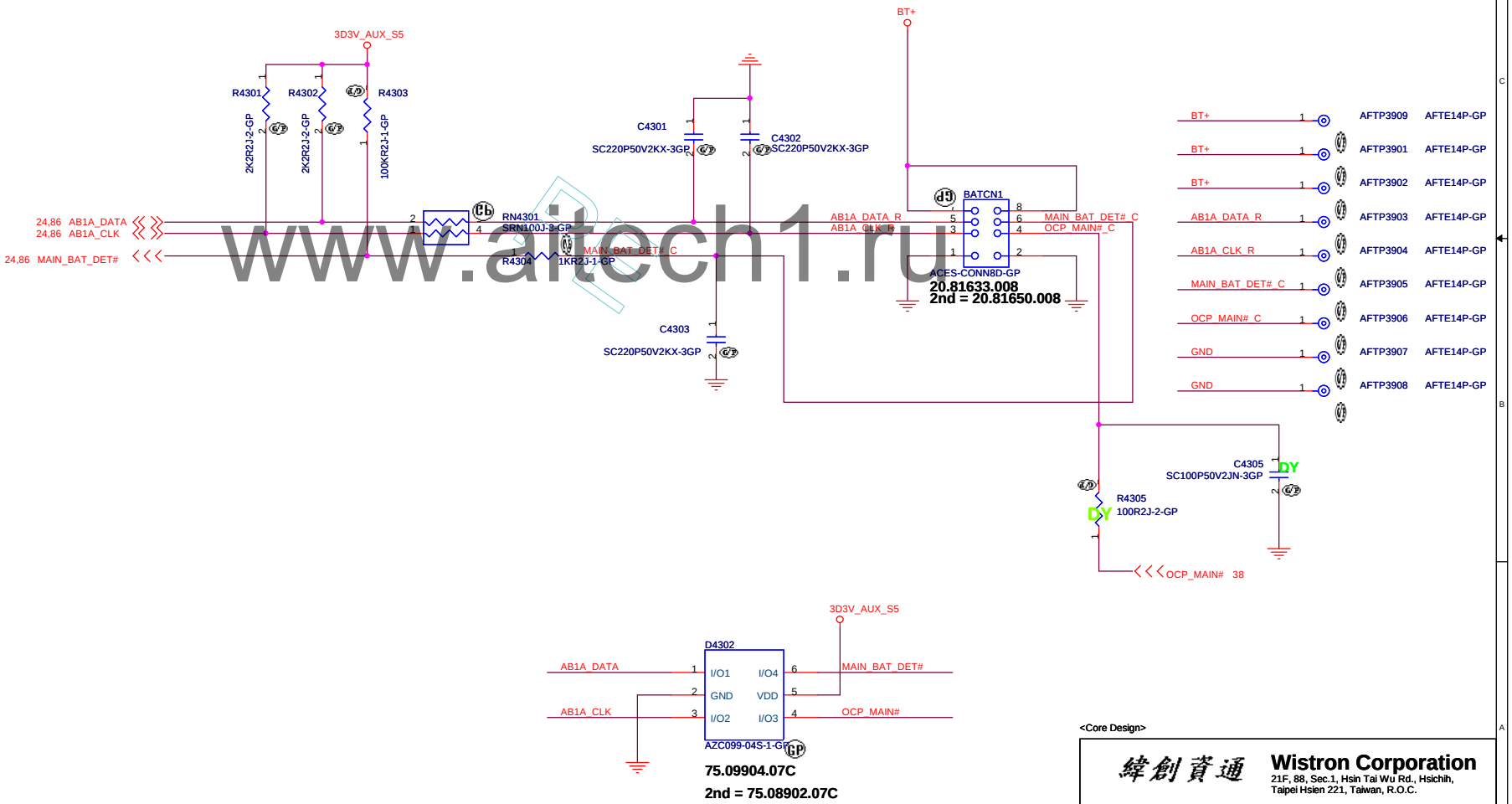
Battery Connector



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Title: **Reserved**

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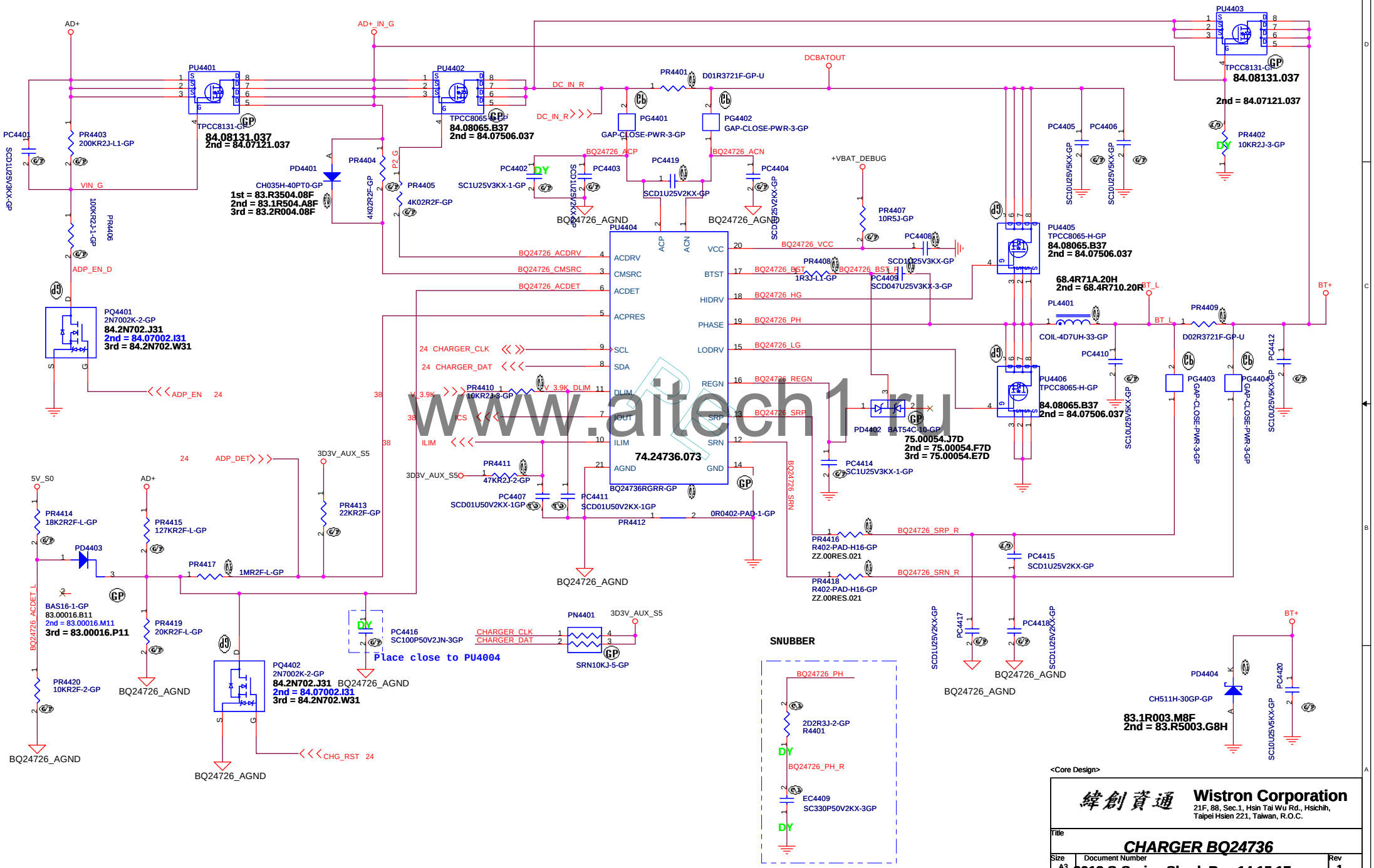
BQ24736 for CHARGER



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Title: **CHARGER BQ24736**

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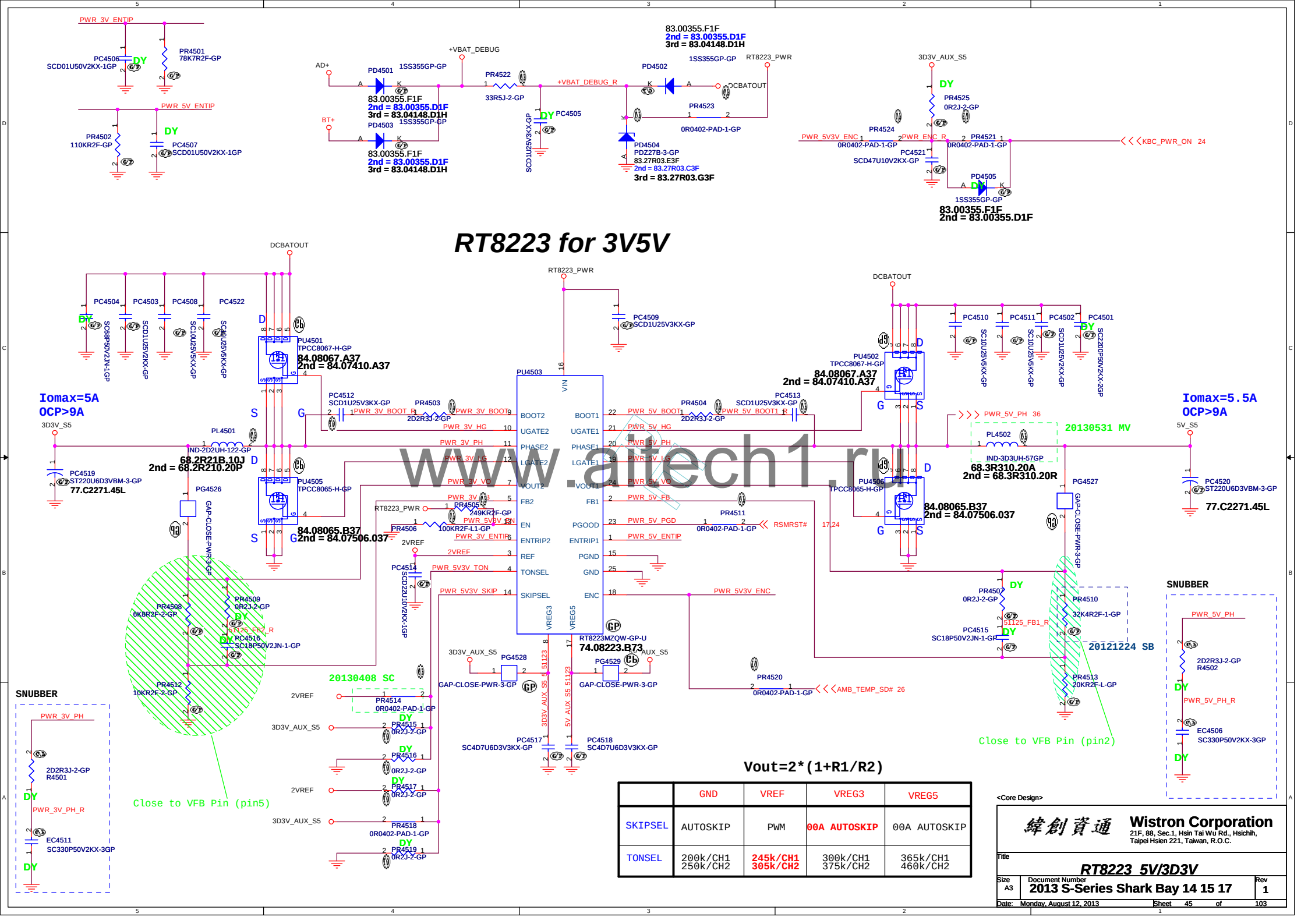

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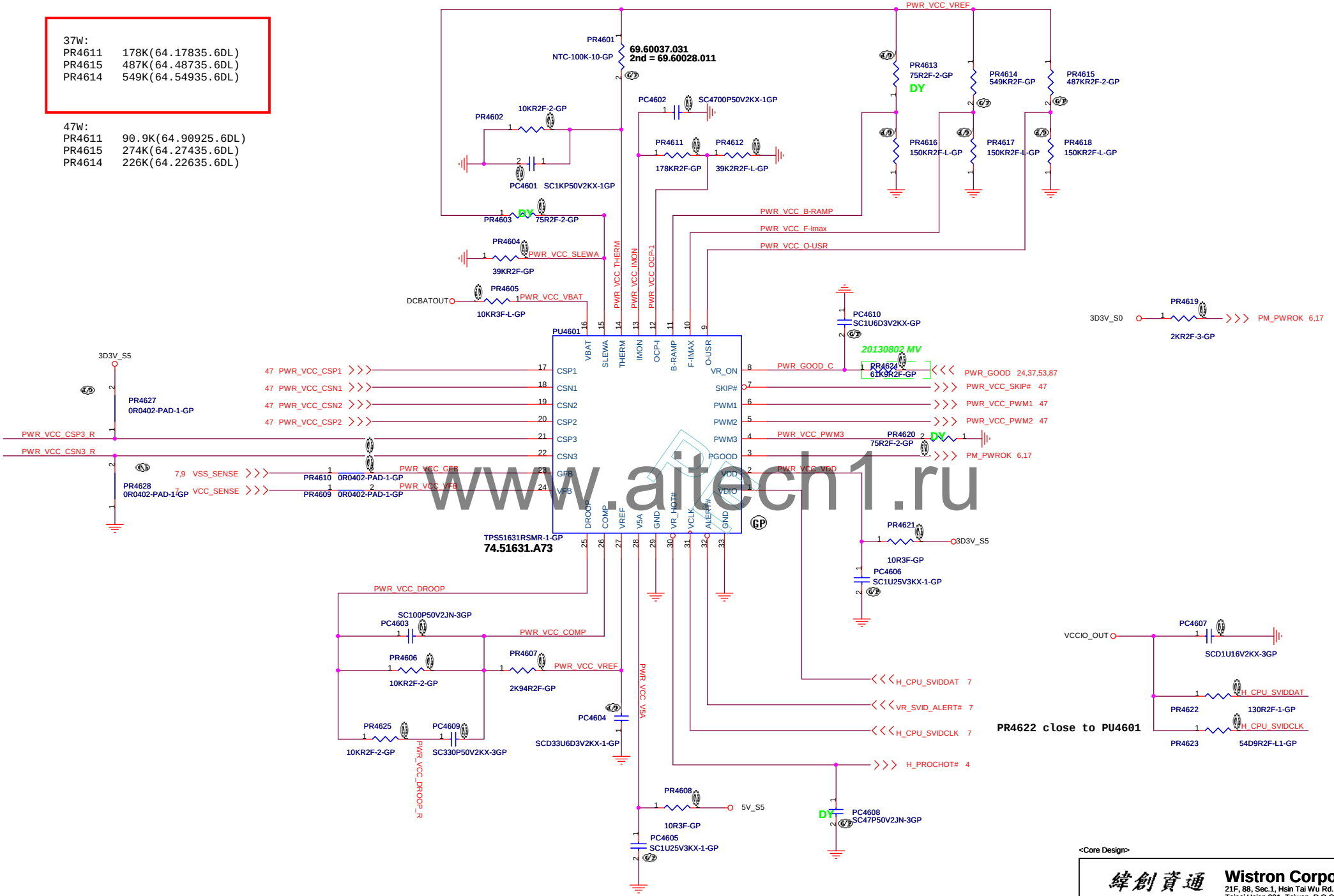
37W:
PR4611 178K(64.17835.6DL)
PR4615 487K(64.48735.6DL)
PR4614 549K(64.54935.6DL)

47W:
PR4611 90.9K(64.90925.6DL)
PR4615 274K(64.27435.6DL)
PR4614 226K(64.22635.6DL)



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Title: TPS51631_CPUCORE(1/2)

Size: A3 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

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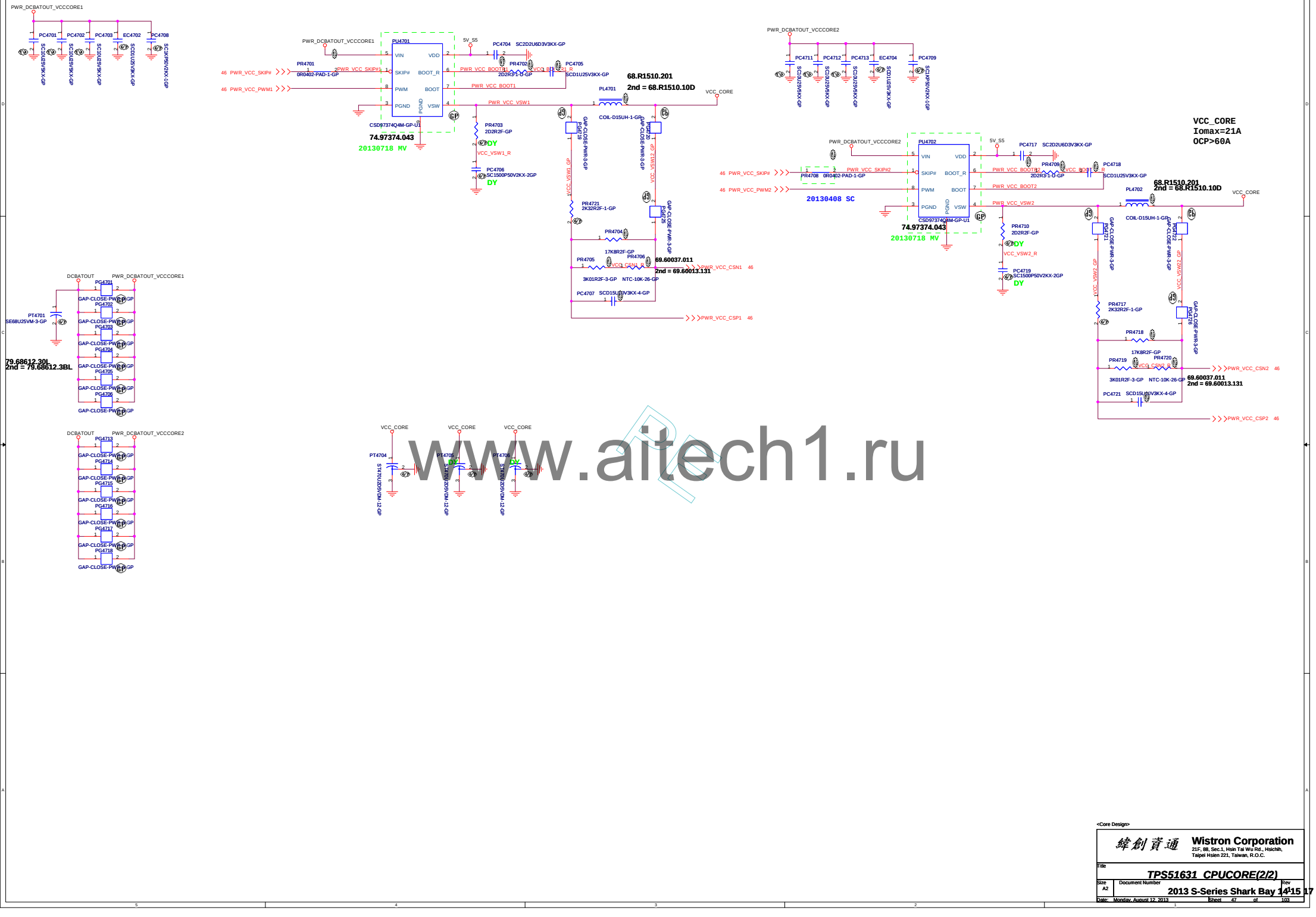

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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51631_CPUCORE(2/2)

Size: A2 | Document Number: 2013 S-Series Shark Bay 14"15 17 | Rev:

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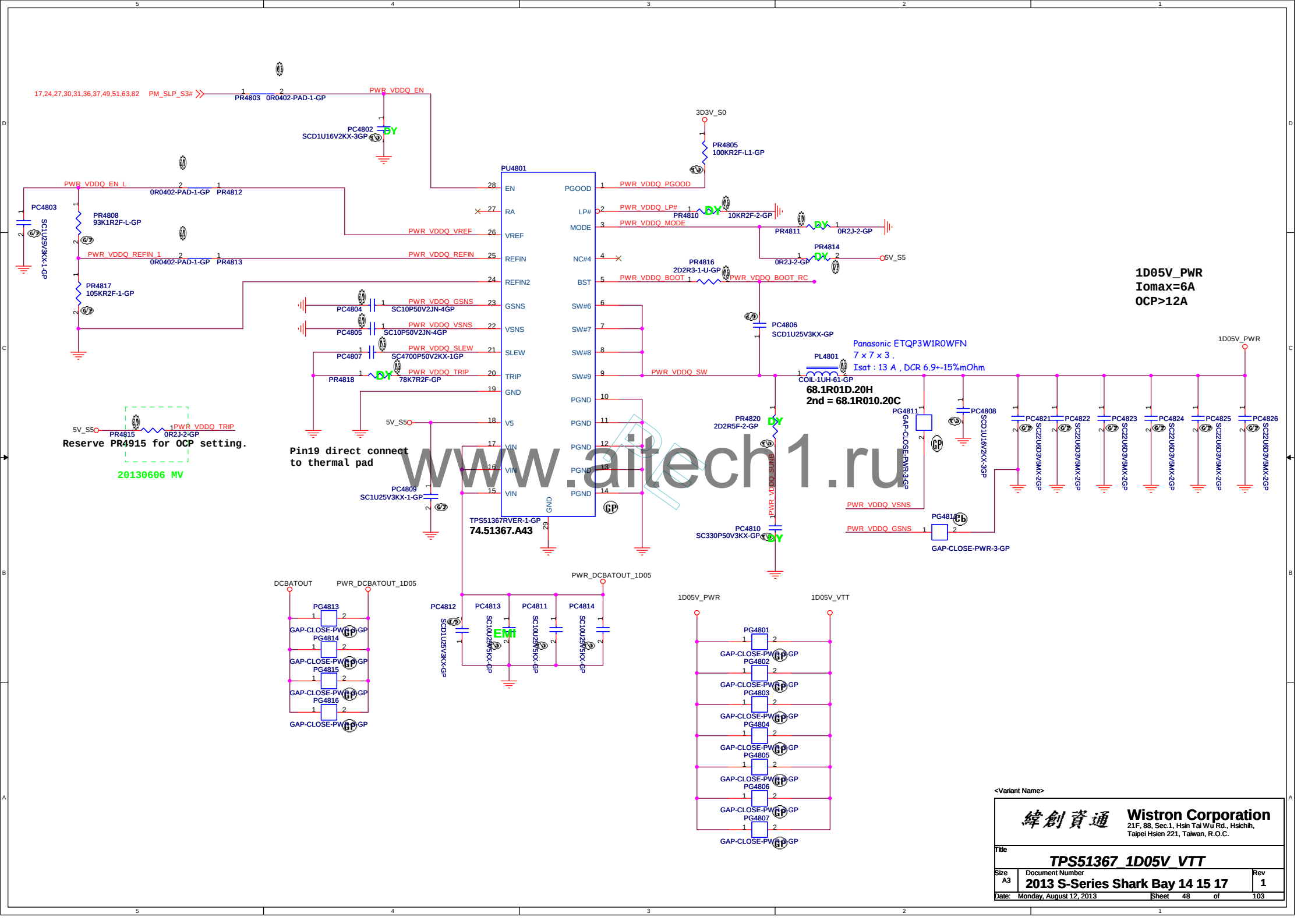

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緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	TPS51367_1D05V_VTT	
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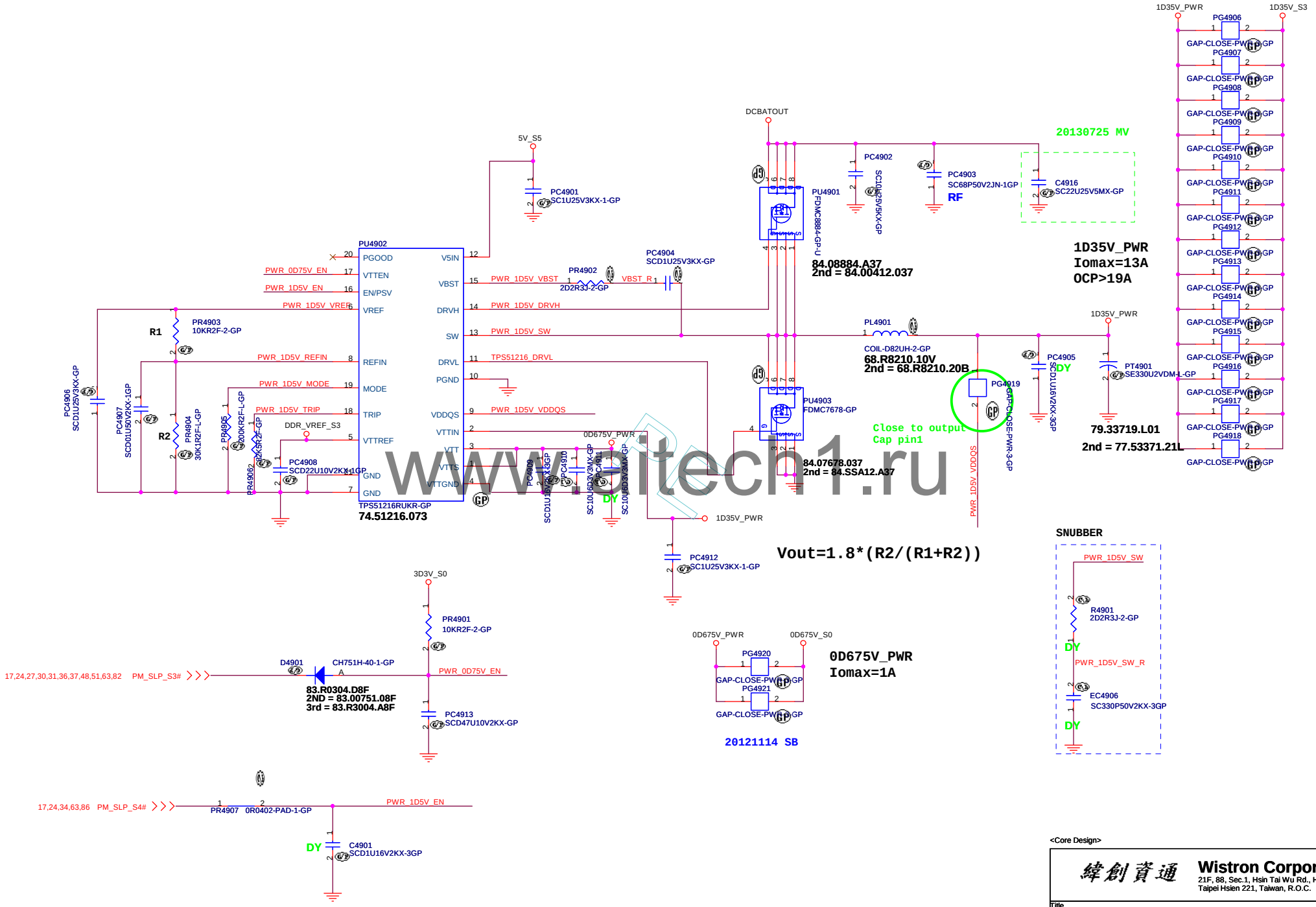

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Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51216_1D35V & 0D675V

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Title

(Reserved)

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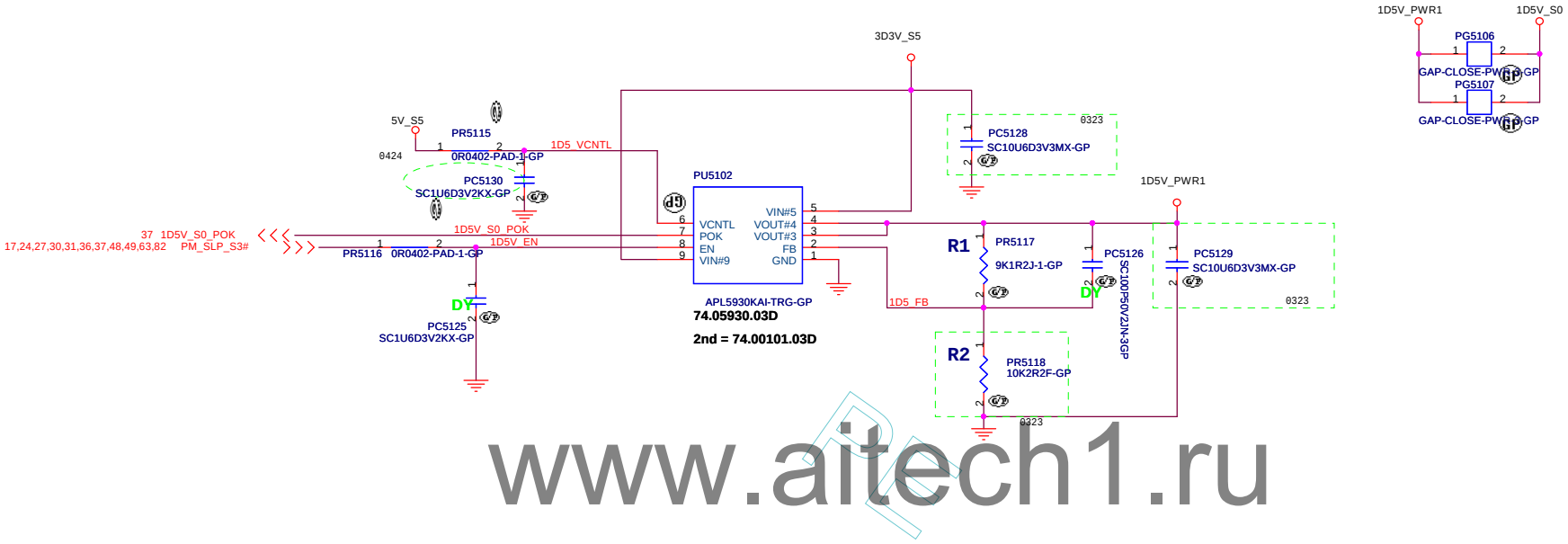

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Title: APL5930_1D5V_S0

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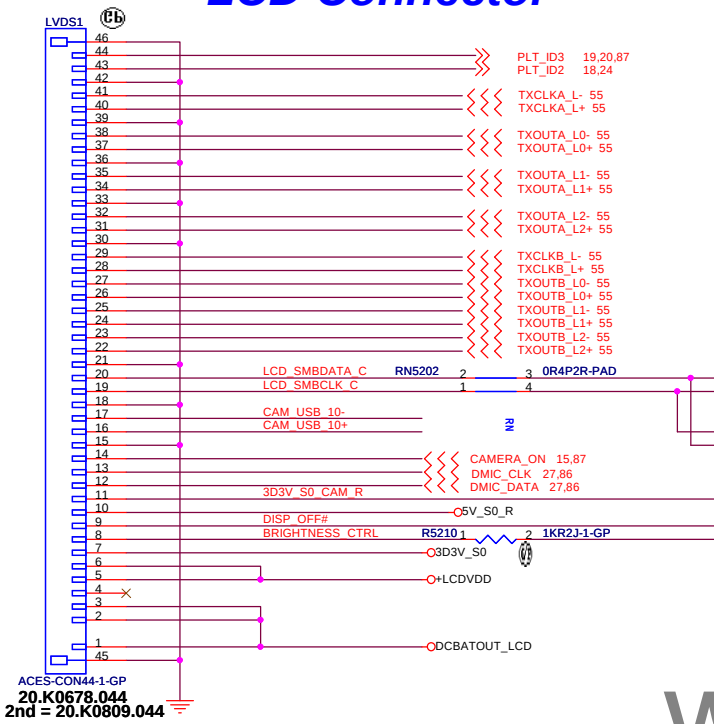
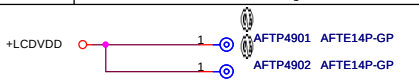
LCD Connector

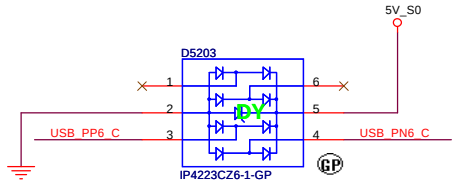


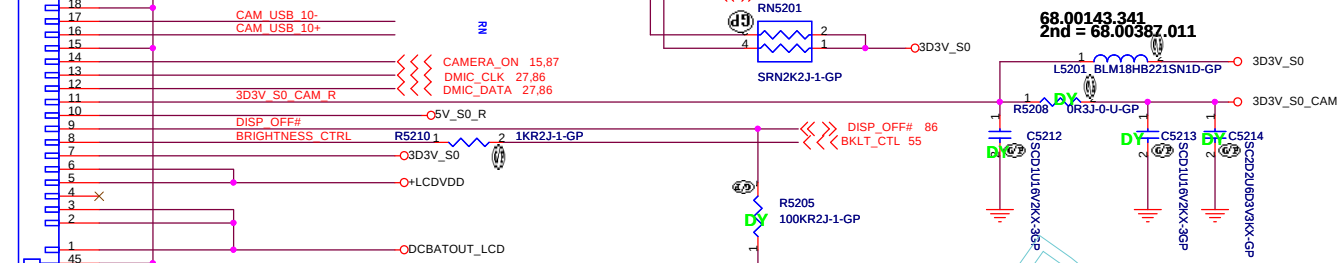
Camera Pin Define

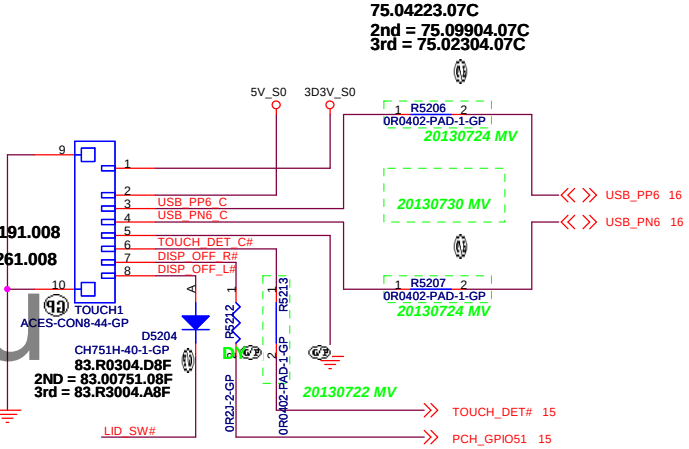
No.	Signal
1	DMIC_CLK
2	DMIC_DATA
3	GND
4	3.3V_MIC
5	5V_KBL
6	EN
7	VCC_5V
8	GND
9	D+
10	D-

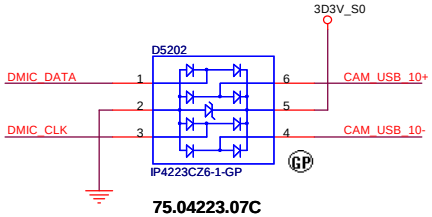
	GPIO23 PLT_ID2	GPIO69 PLT_ID3
Rampage 14"	0	1
Renegade 15"	1	0
Ricochet 17"	1	1

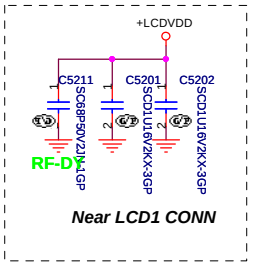


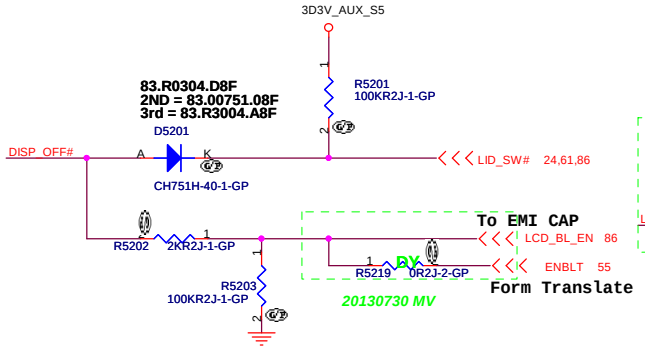


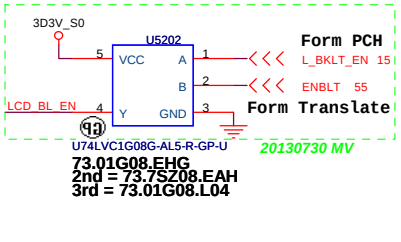


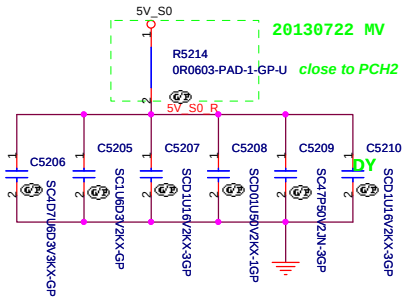




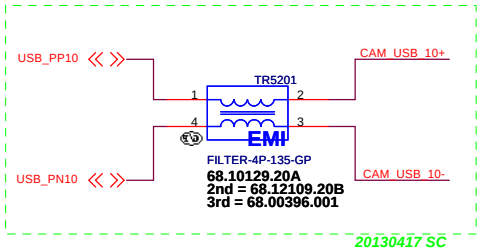




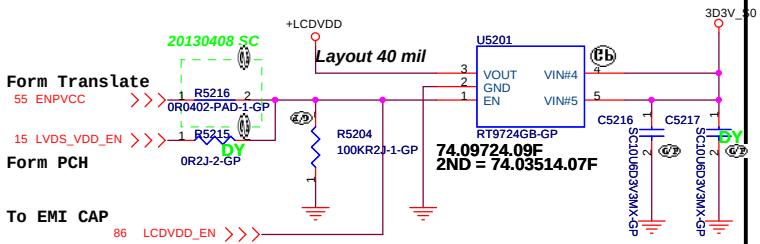




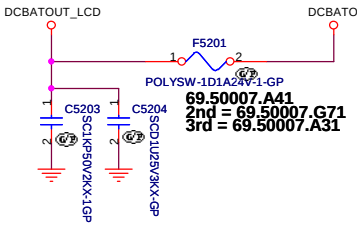
CAMERA



LCD POWER CIRCUIT



LED BACKLIGHT CONVERTER POWER



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Title: LCD Connector

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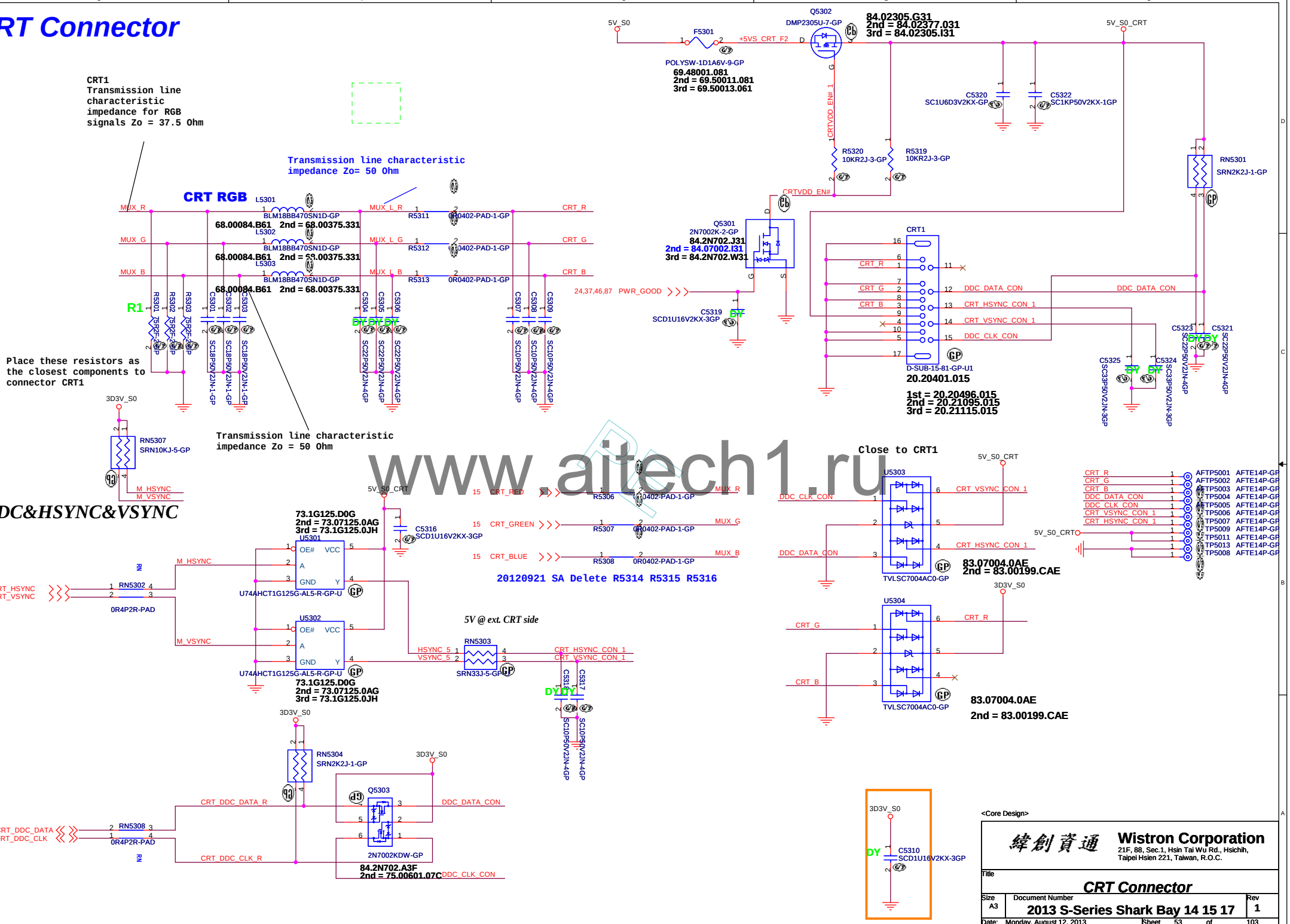
CRT Connector



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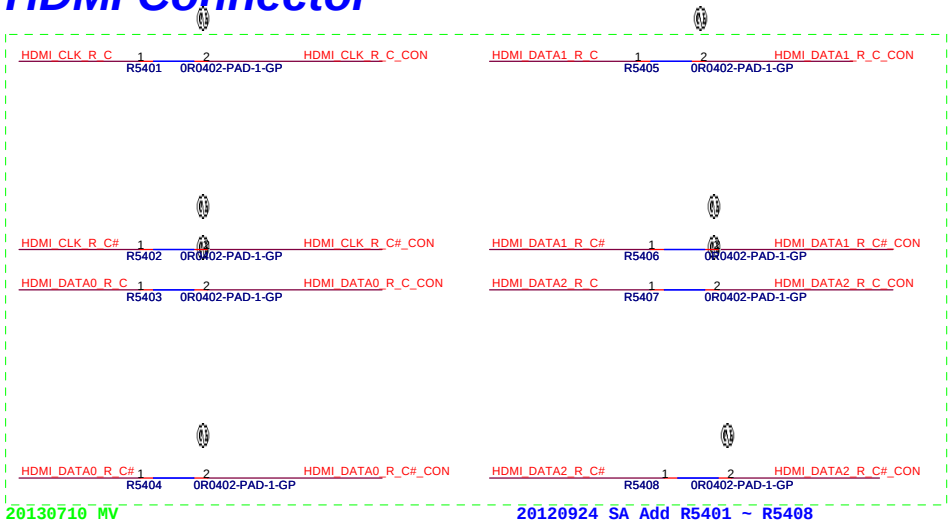
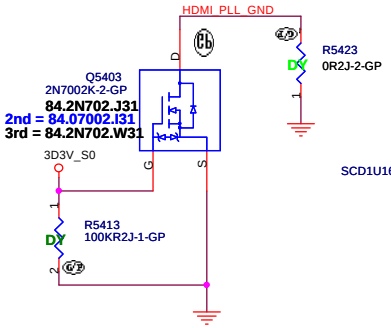
HDMI Connector

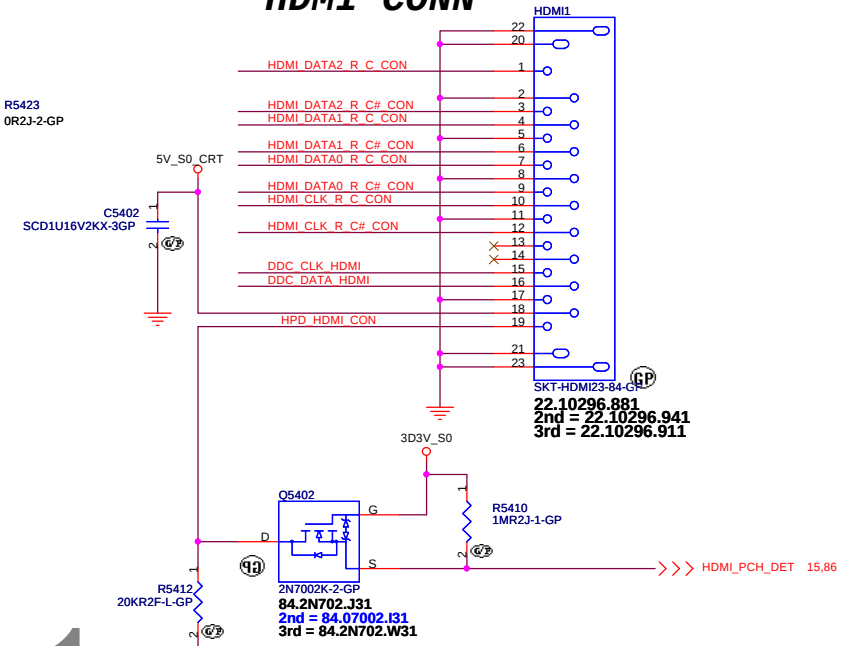


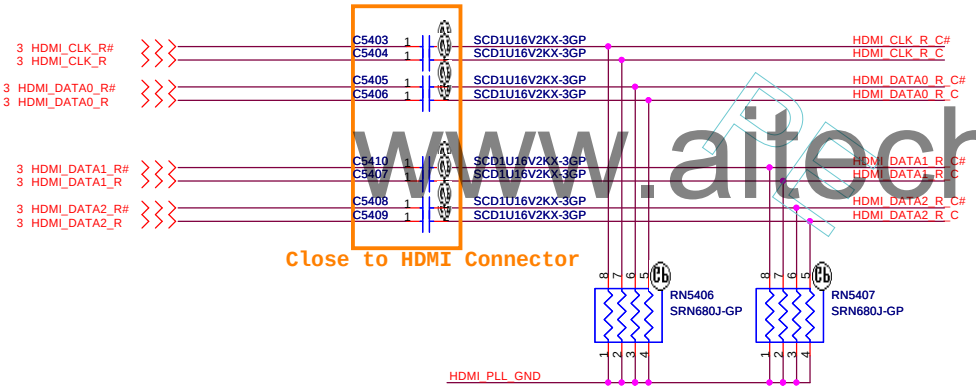
20130710 MV

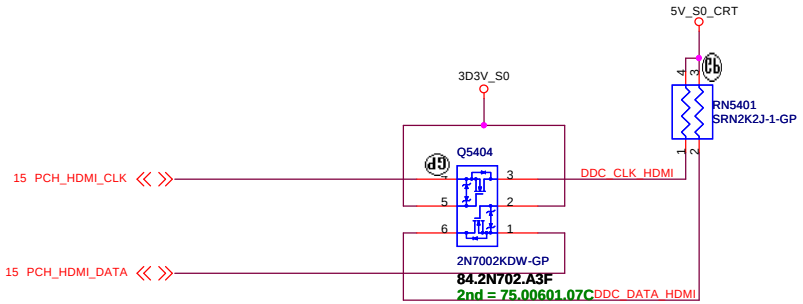
20120924 SA Add R5401 ~ R5408



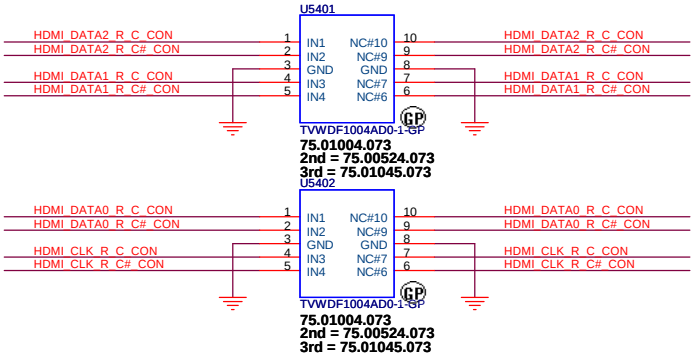
HDMI CONN







Close to HDMI1



www.aitech1.ru

Routing Guidelines:
CTRLDATA must be routed longer than CTRLCLK within 1000 mils (25.4 mm).
The total delay on CTRLDATA should be longer than CTRLCLK.

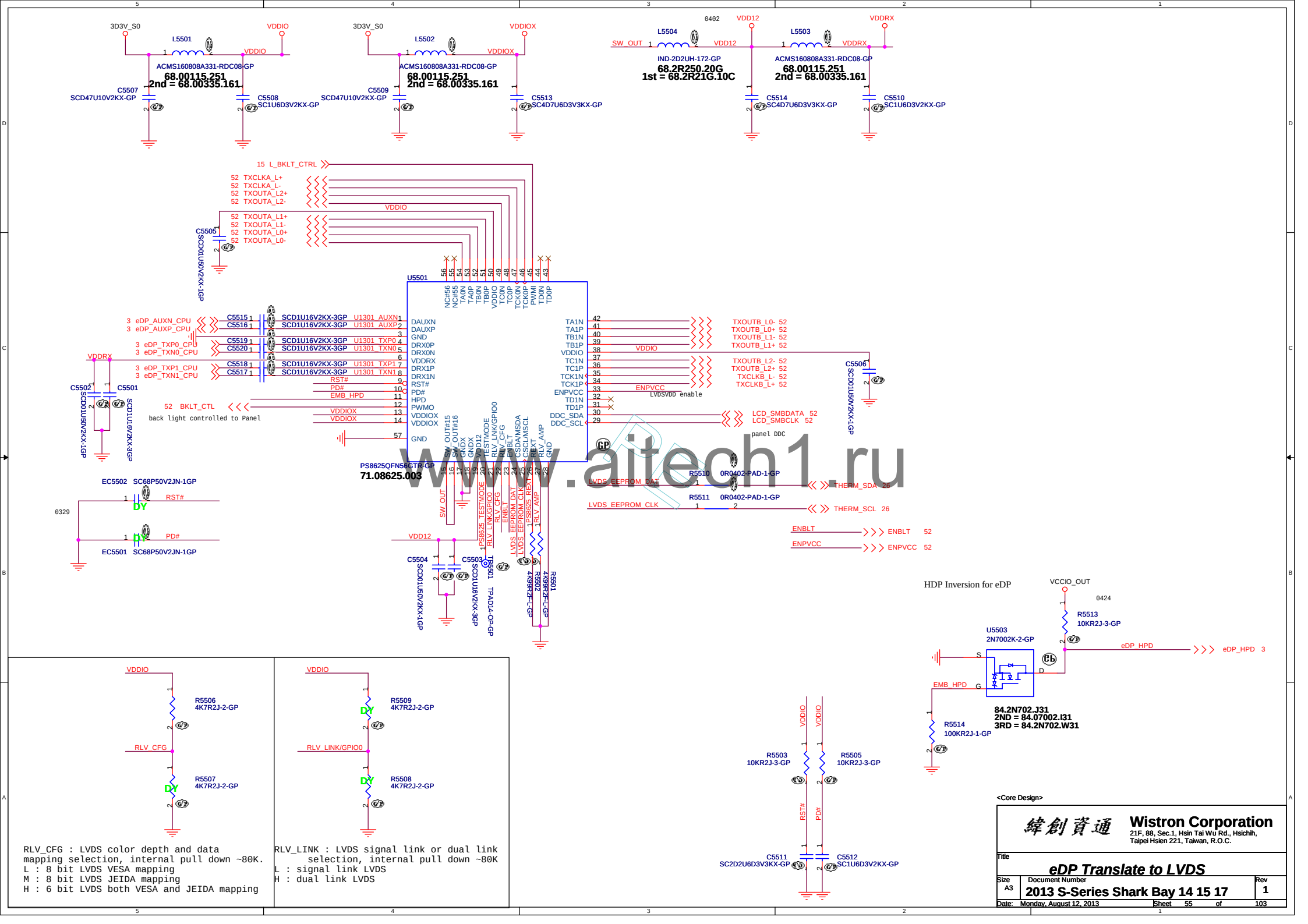
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDMI Level Shifter/Conn**

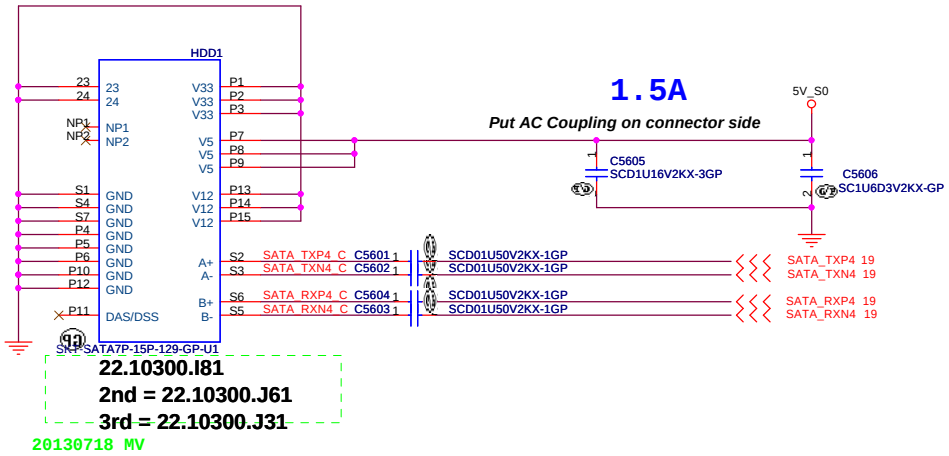
Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

Date: Monday, August 12, 2013 Sheet 54 of 103



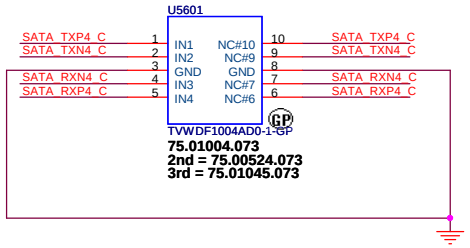
www.aitech1.ru

HDD Connector



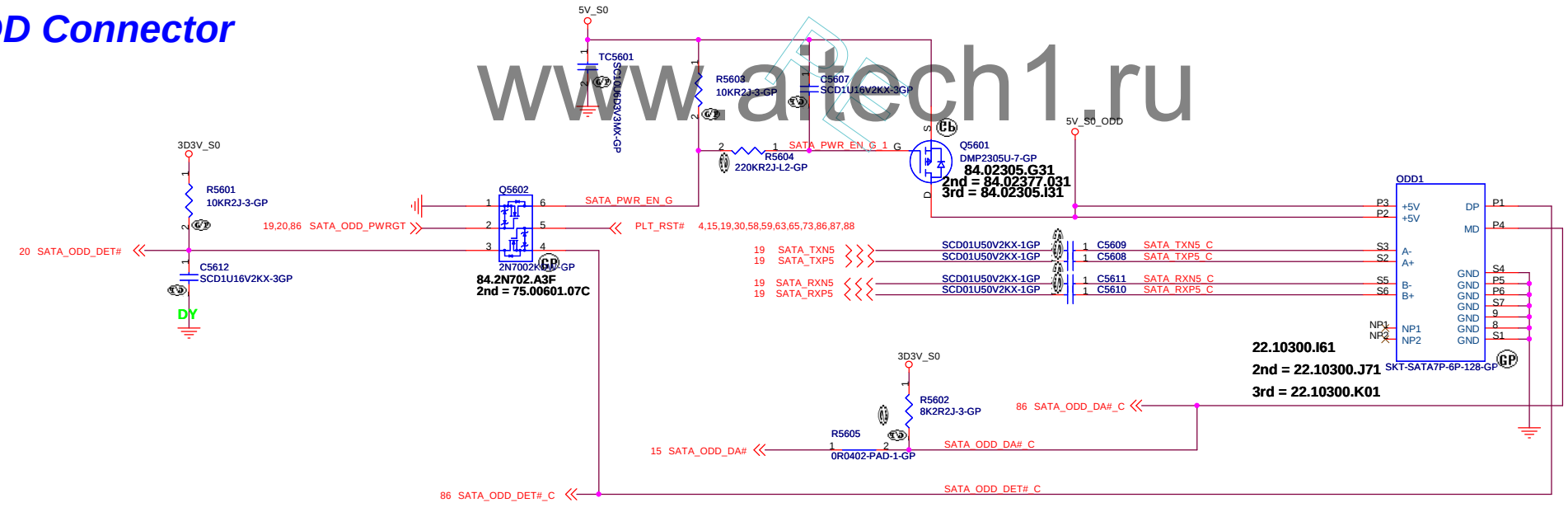
Ultra Low Capacitance TVS Arrays
(Pin5.6.7.8 No Internal Connection)

EMI Cap.



ODD Connector

www.altech1.ru



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

Date: Monday, August 12, 2013 Sheet 56 of 103

(Blanking)

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

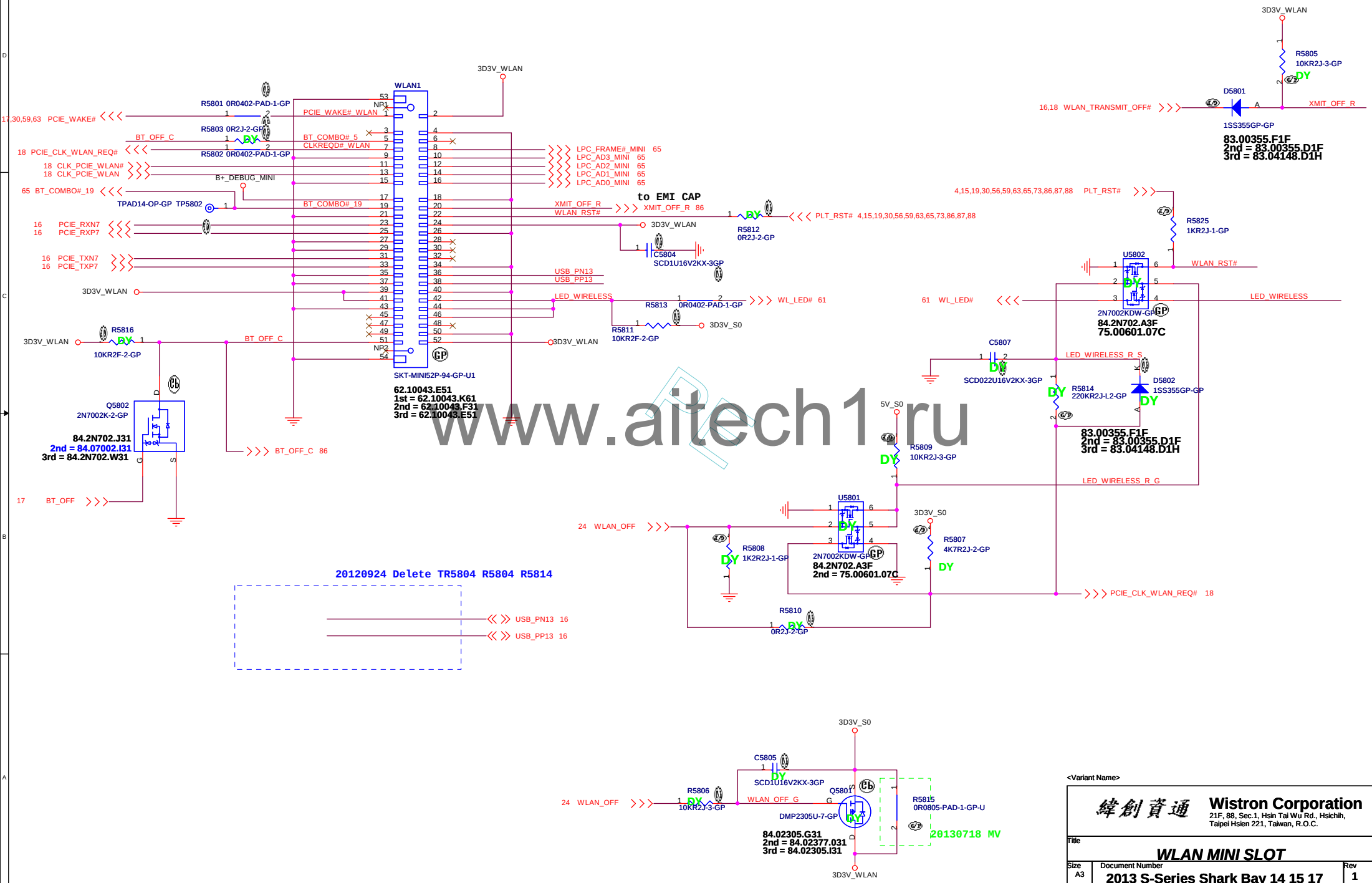
Title: *(Reserved)*

Size: A3 | Document Number: 2013 S-Series Shark Bay 14"15 17 | Rev: 1.1

Date: Wednesday, July 03, 2013 | Sheet 57 of 103

WLAN Connector

Mini-Card--WLAN (Half)



www.aitech1.ru

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: WLAN MINI SLOT

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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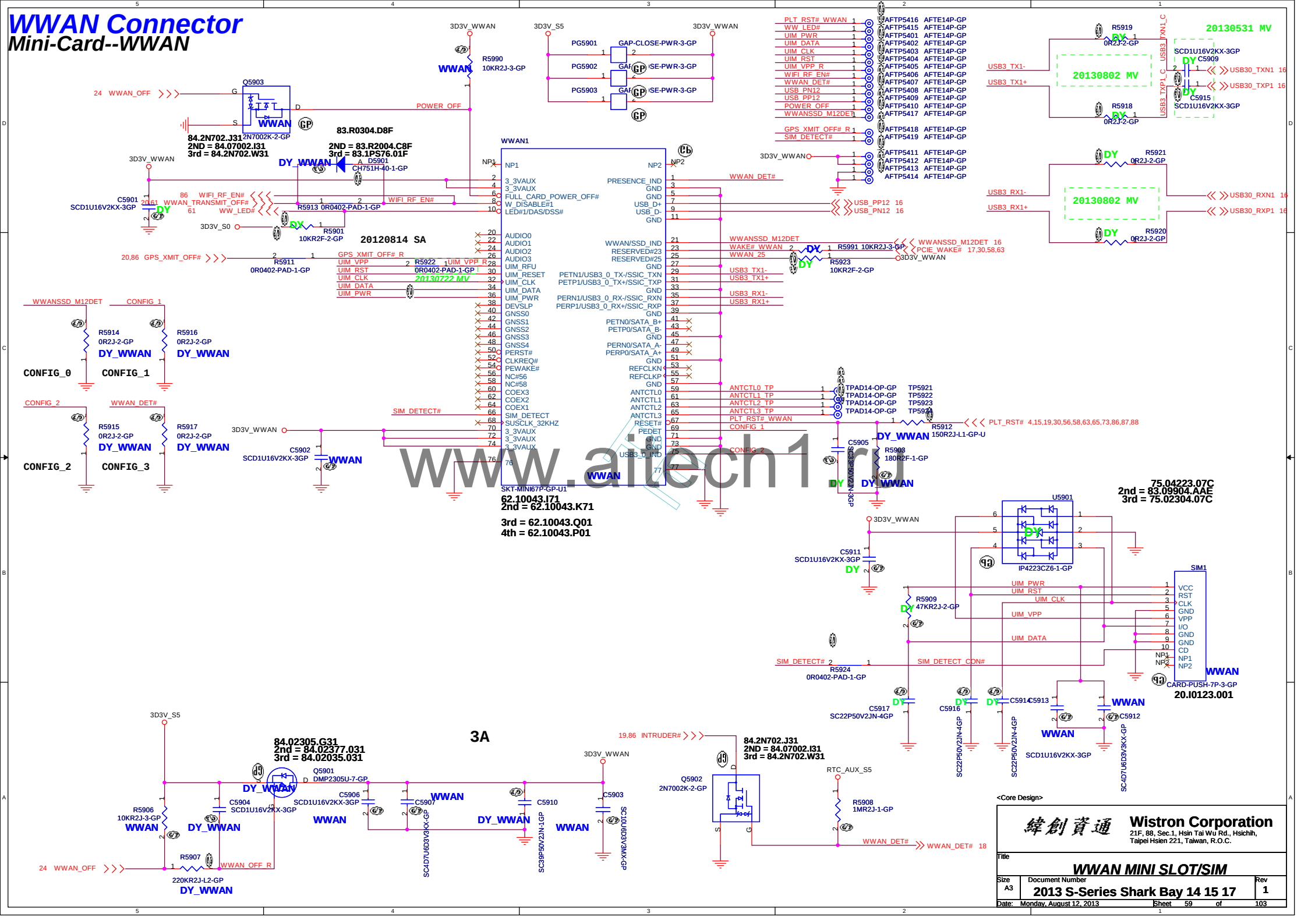
WWAN Connector
Mini-Card--WWAN



www.aitech1.ru

www.aitech1.ru

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Flash***

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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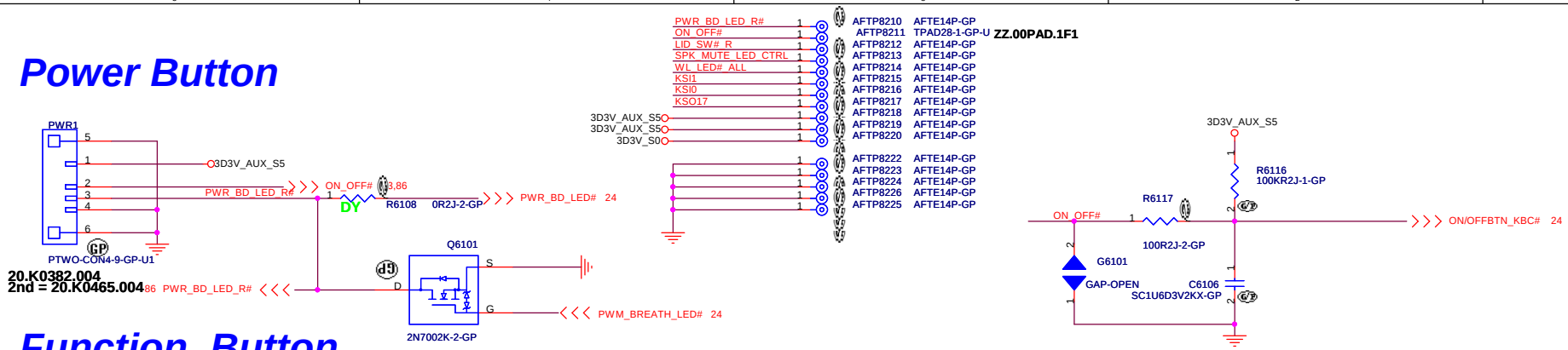
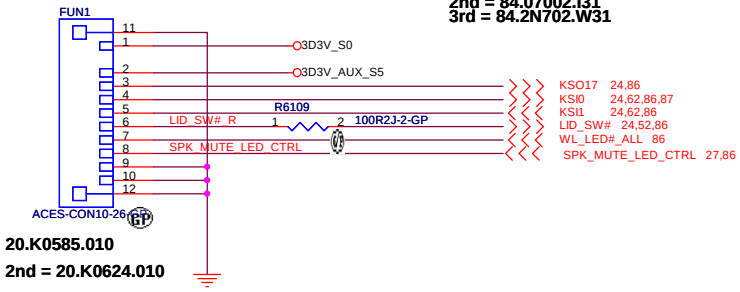
Power Button



Function Button



84.2N702.J31
2nd = 84.07002.I31
3rd = 84.2N702.W31

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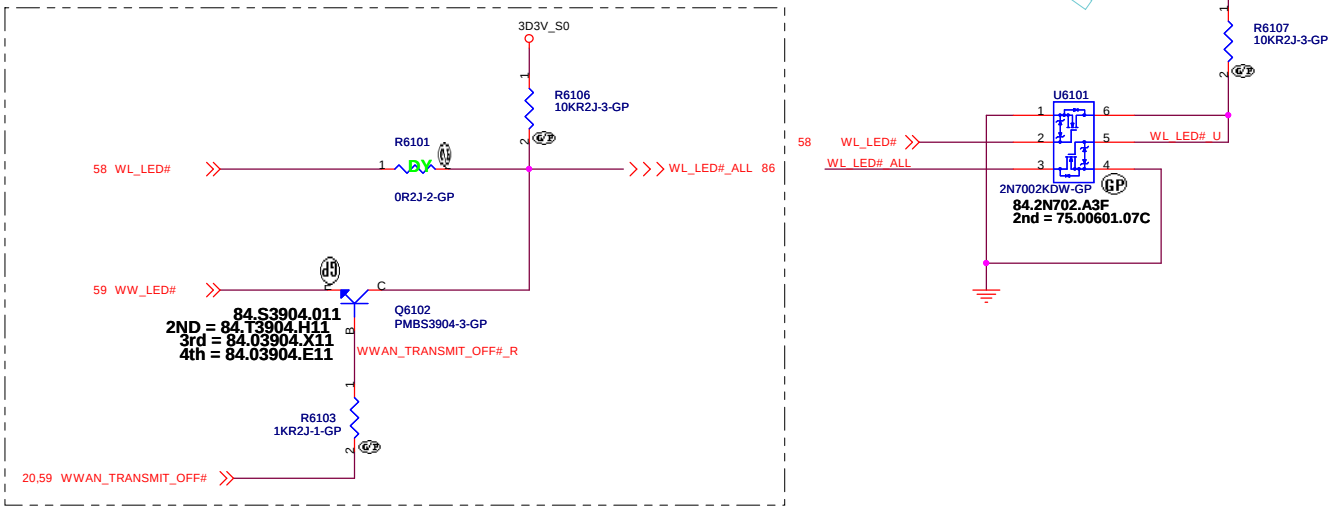
WLAN / WWAN POWER LED



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Bard/Power Button

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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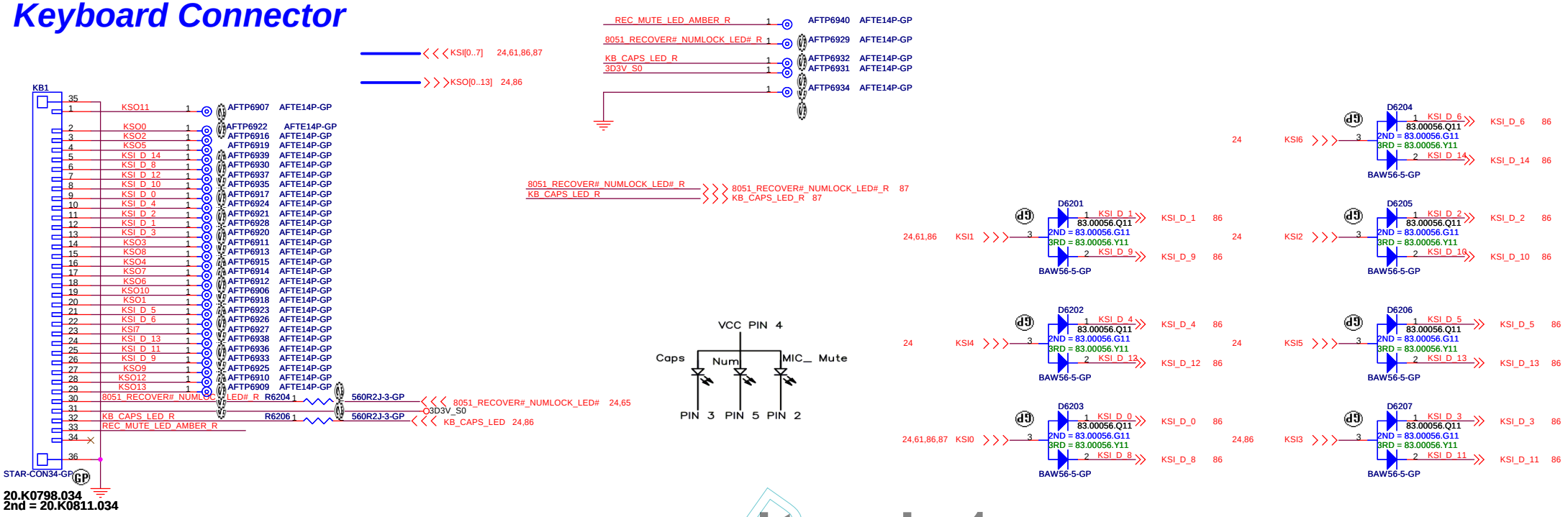
Keyboard Connector



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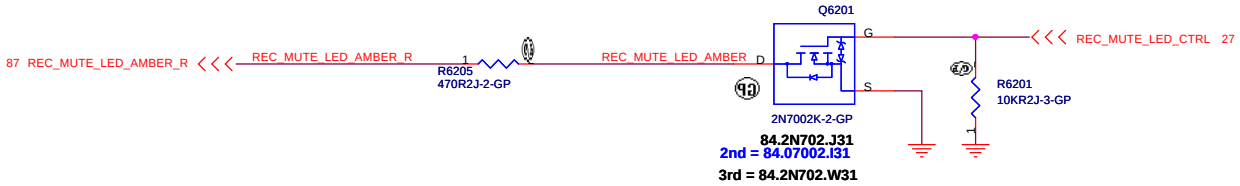
On Keyboard LEDs

<MUTE> Internal MIC ON= No light; OFF/Mute= Amber



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Key Board/Touch Pad**

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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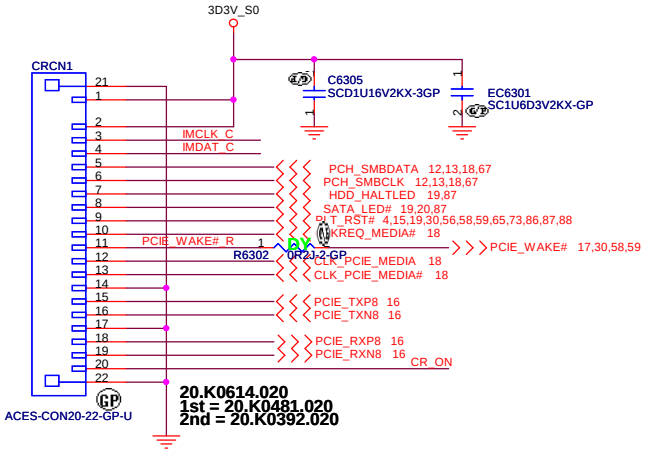
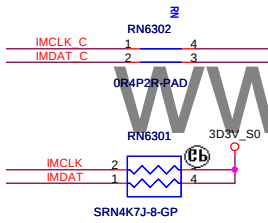
Audio Board +Touch Pad + Card Reader IC Connector



PCIE_WAKE# 1 AFTP3127 AFTE14P-GP
CR_ON 1 AFTP3126 AFTE14P-GP

Fiji and Python no this function
Please connect to pin 11 pin20

PCH_SMBDATA 1 AFTP3134 AFTE14P-GP
PCH_SMBCLK 1 AFTP3110 AFTE14P-GP
PLT_RST# 1 AFTP3108 AFTE14P-GP
CLKREQ_MEDIA# 1 AFTP3109 AFTE14P-GP
CLK_PCIE_MEDIA 1 AFTP3111 AFTE14P-GP
CLK_PCIE_MEDIA# 1 AFTP3112 AFTE14P-GP
PCIE_TXP8 1 AFTP3113 AFTE14P-GP
PCIE_TXN8 1 AFTP3114 AFTE14P-GP
PCIE_RXP8 1 AFTP3115 AFTE14P-GP
PCIE_RXN8 1 AFTP3116 AFTE14P-GP
HDD_HALTLED 1 AFTP3117 AFTE14P-GP
SATA_LED# 1 AFTP3118 AFTE14P-GP
IMCLK_C 1 AFTP3120 AFTE14P-GP
IMDAT_C 1 AFTP3121 AFTE14P-GP
3D3V_S0 1 AFTP3122 AFTE14P-GP
3D3V_S0 1 AFTP3123 AFTE14P-GP
1 AFTP3124 AFTE14P-GP
1 AFTP3125 AFTE14P-GP



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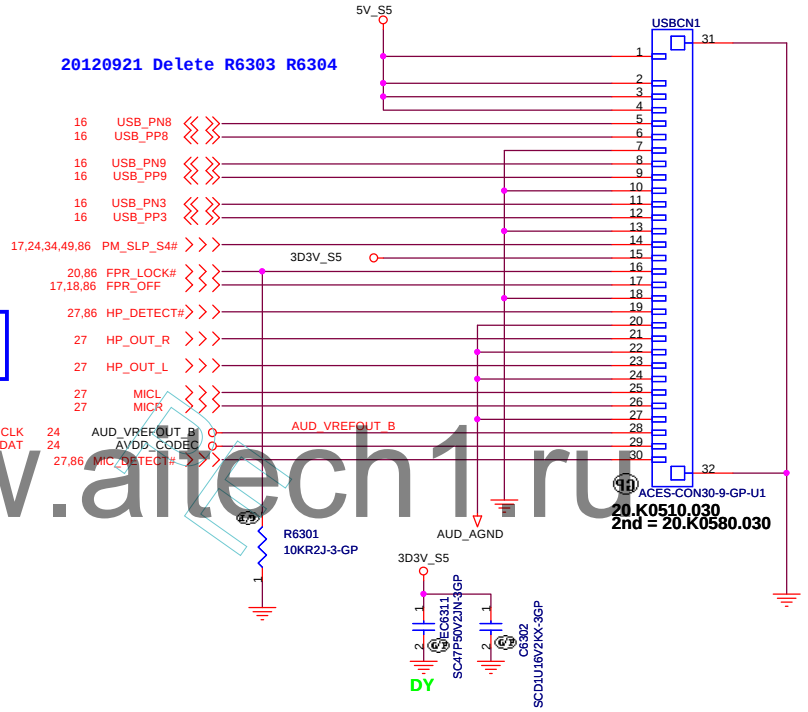
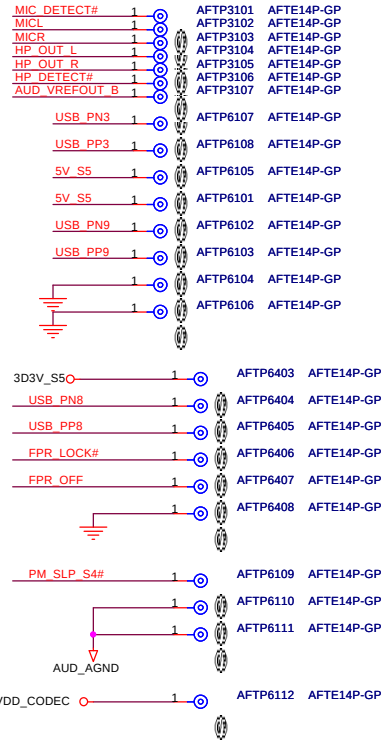
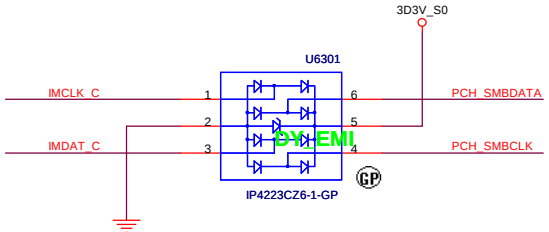
Right Side Audio & FP & USB Connector

20120921 Delete R6303 R6304





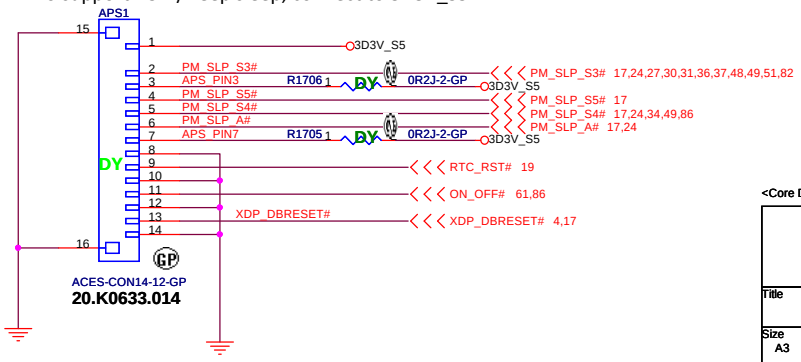


Pinout on customer's board,
as in the PDG, CDI #486713,

Pin	Signal Name
1	VccSus3_3
2	SLP_S3#
3	VccDSW3_3
4	SLP_S5#
5	SLP_S4#
6	SLP_A#
7	+V3.3DS
8	GND
9	RTCRST#
10	GND
11	PWRBTN#
12	GND
13	SYS_RESET#
14	GND

APS1 for QT test do not install

No support DSW/Deep sleep, connect to 3D3V_S5



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM3,4 (2/4)

Size	Document Number	Rev
A2	2013 S-Series Shark Bay 14/15/17	

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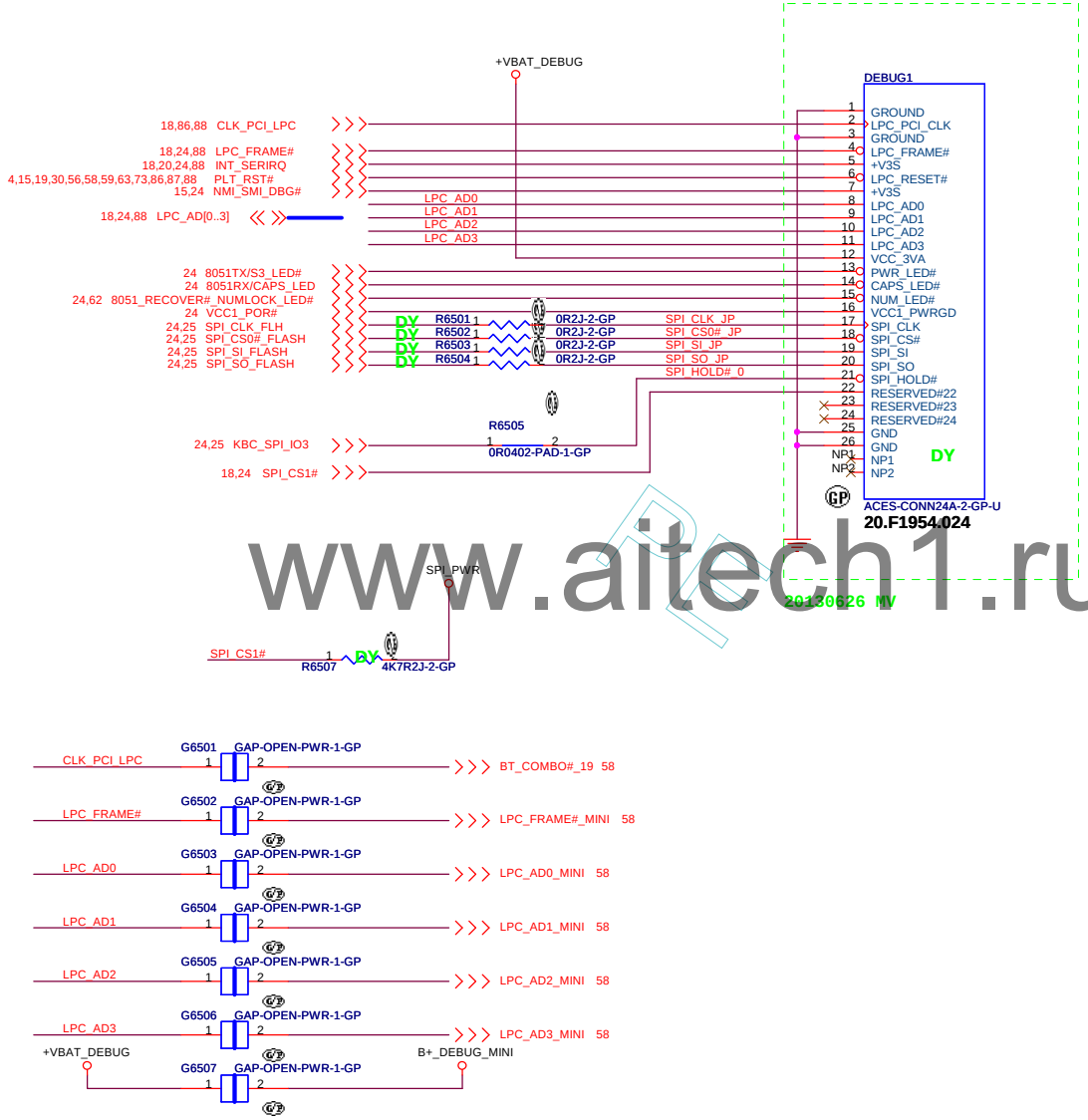
24 PIN LPC DEBUG CONN.



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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug connector***

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

Date: Monday, August 12, 2013 Sheet 65 of 103

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SENSOR HUB

Size: A3 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

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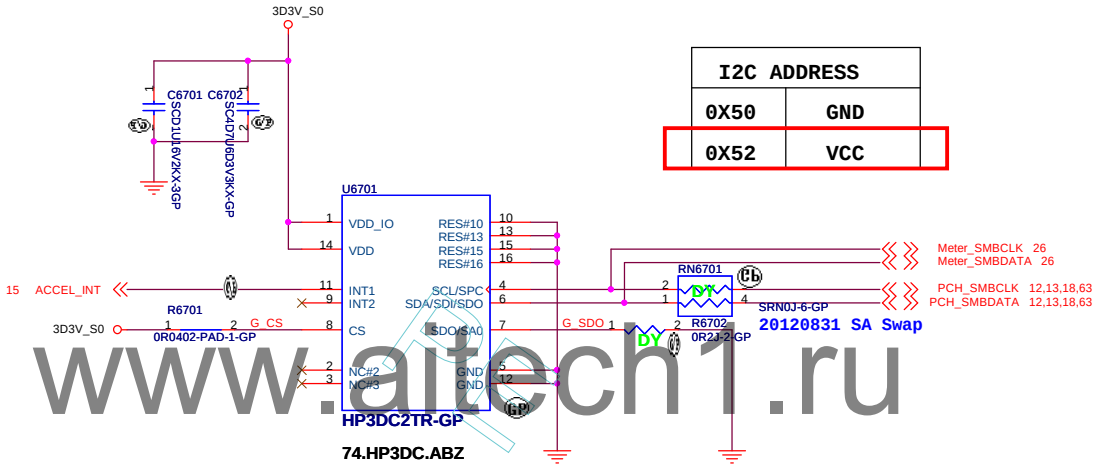
ACCELEROMETER



I2C ADDRESS	
0X50	GND
0X52	VCC

Must be placed in the center of the system

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***G Sensor***

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Thunderbolt (1/5)***

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

Date: Wednesday, July 03, 2013 Sheet 68 of 103

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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Thunderbolt (2/5)***

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

Date: Wednesday, July 03, 2013 Sheet 69 of 103

(Blanking)

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Thunderbolt (3/5)*

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Thunderbolt (4/5)*

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

Date: Wednesday, July 03, 2013 Sheet 71 of 103

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Thunderbolt (5/5)***

Size	Document Number	Rev
A2	2013 S-Series Shark Bay 14 15 17	1

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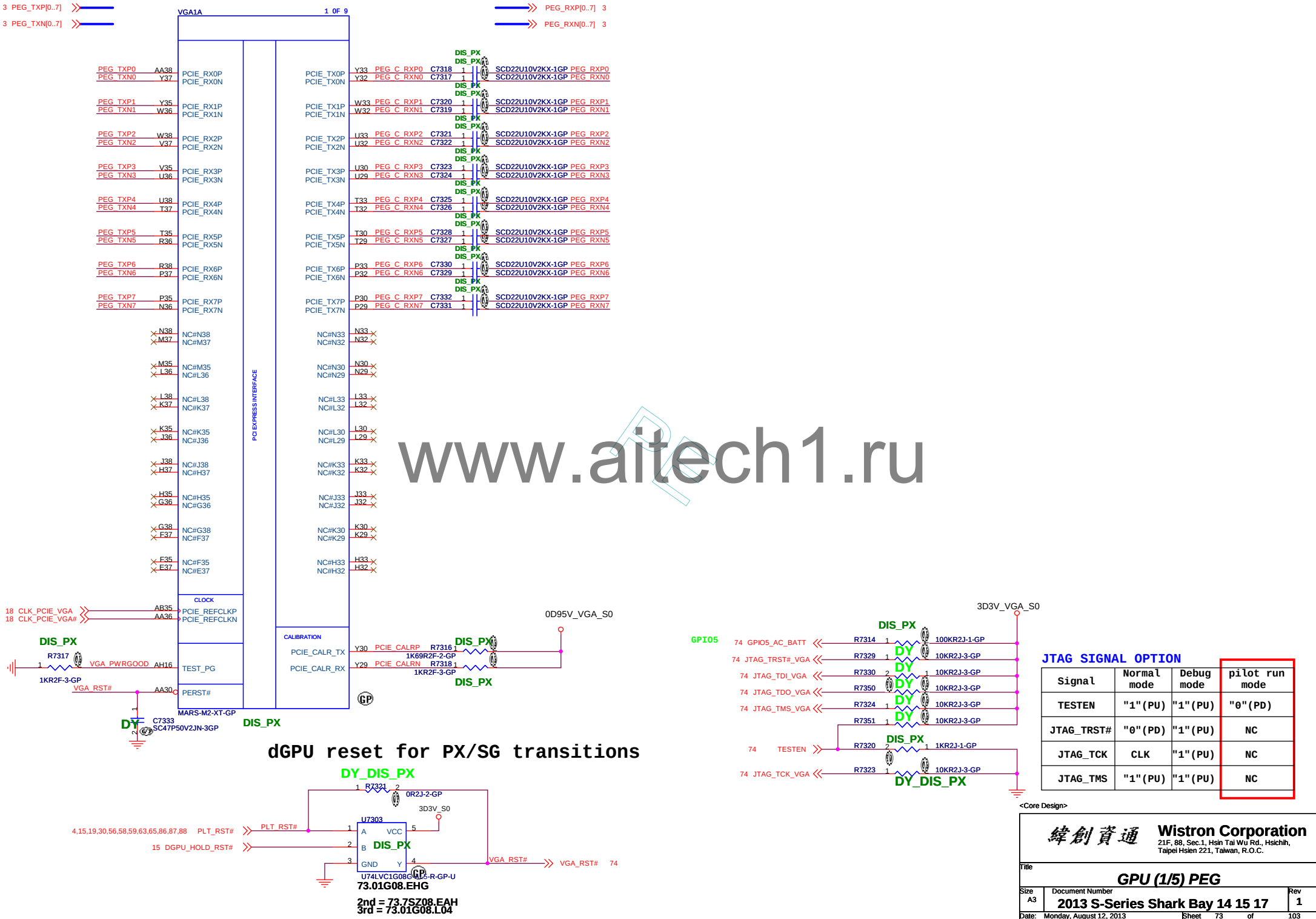

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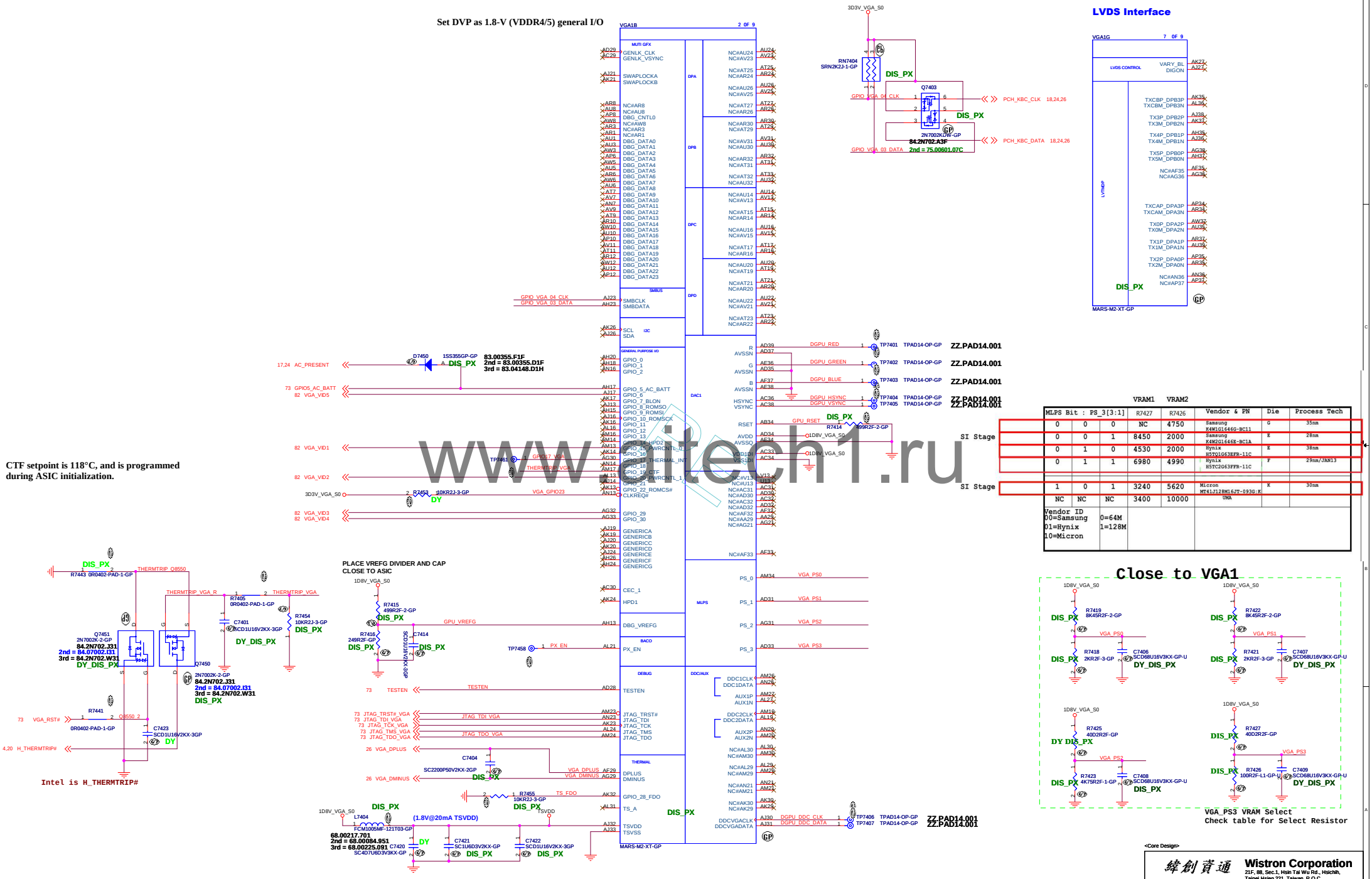
Set DVP as 1.8-V (VDDR4/5) general I/O

CTF setpoint is 118°C, and is programmed during ASIC initialization.



www.itech1.ru

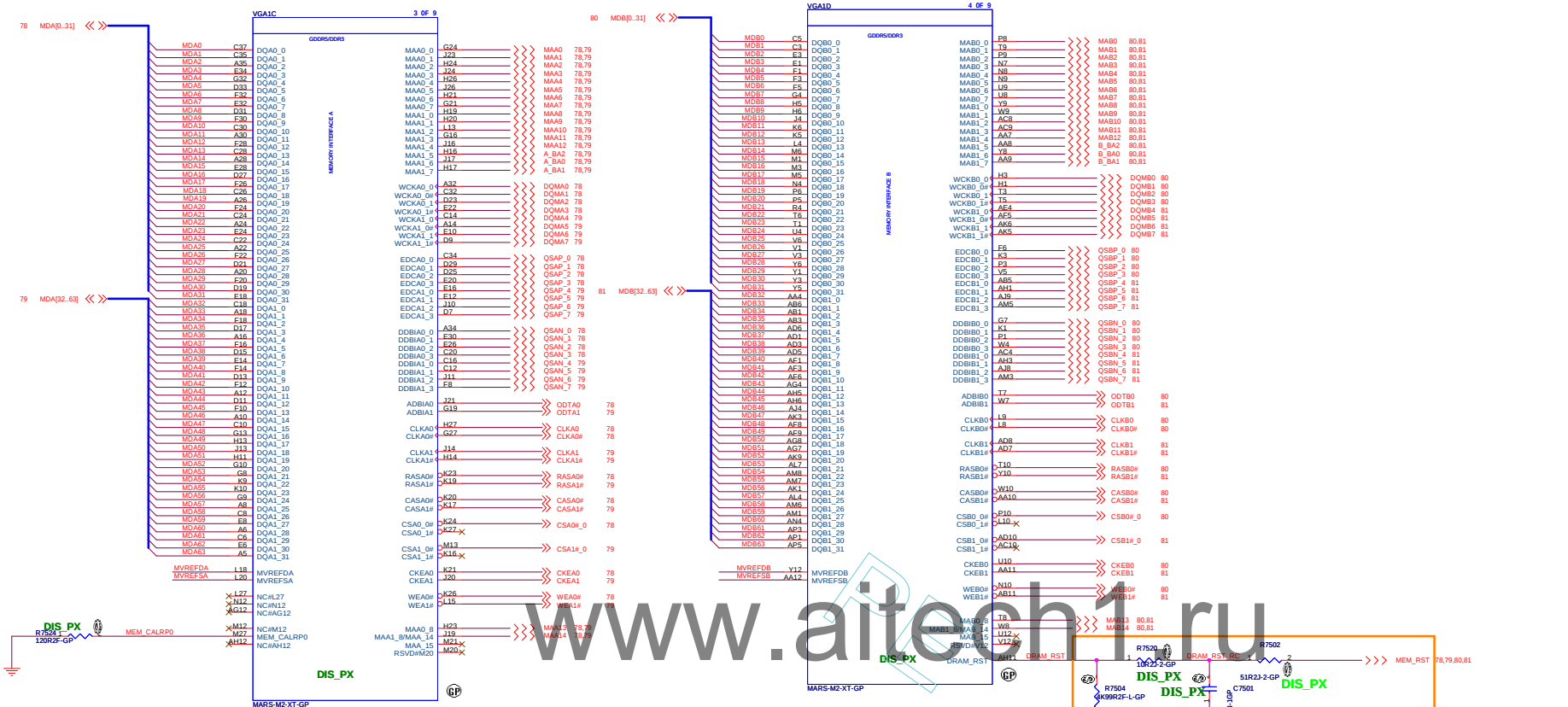
<Core Design>

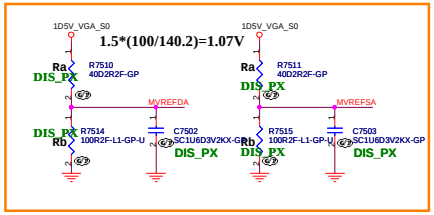
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

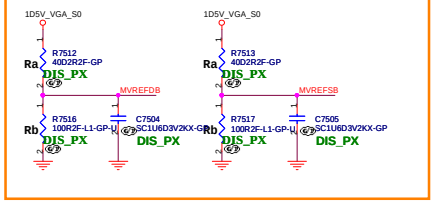
Title: GPU (2/5) DIGITALOUT

Size: A2 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

Date: Monday, August 12, 2013 | Sheet 74 of 103







This basic topology should be used for DRAM_RST for DDR3/GDDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

DDR3/GDDR3 Memory Stuff Option(Mad/Park)

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

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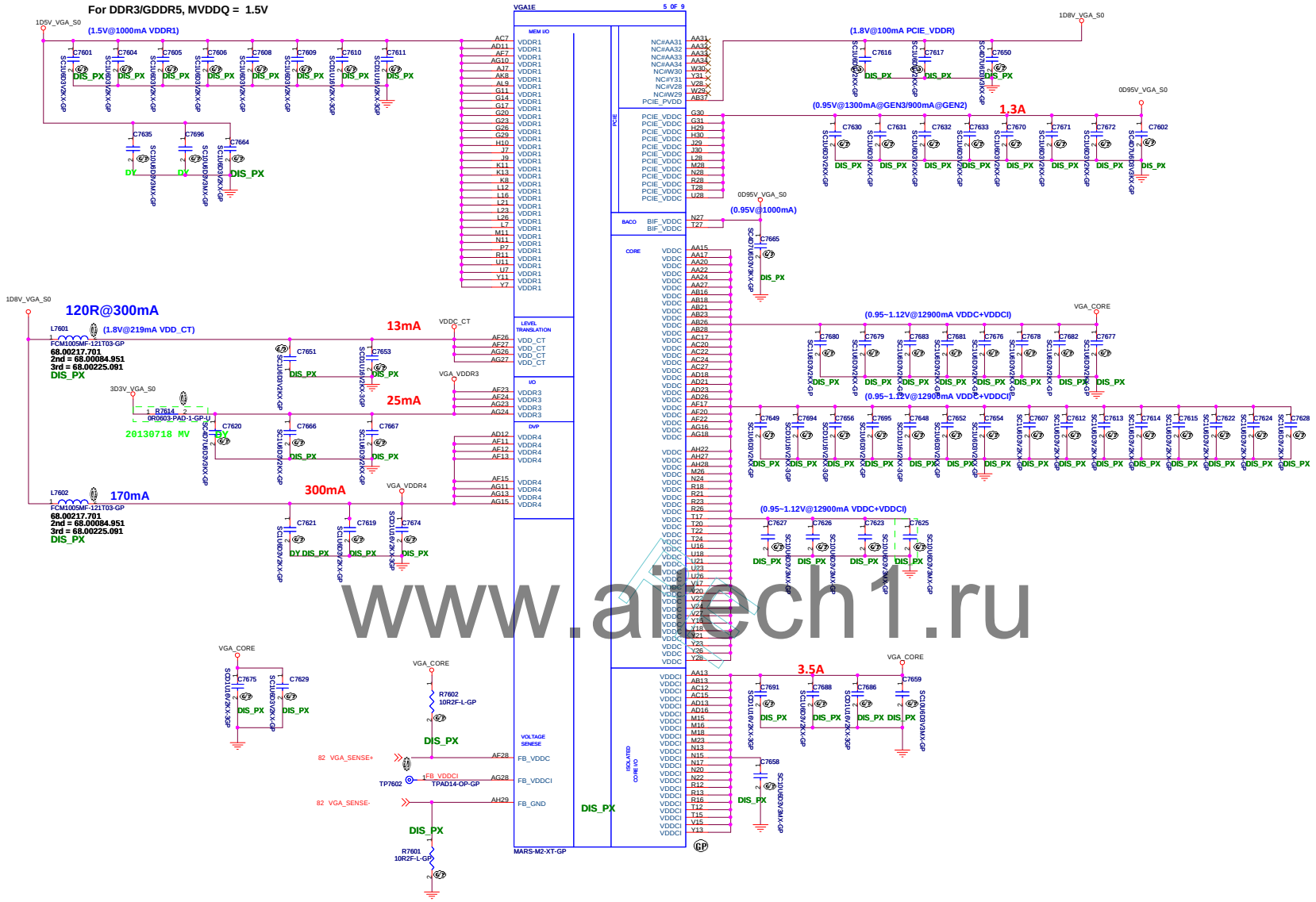
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (3/5) VRAM I/F

Size	Document Number	Rev
A2	2013 S-Series Shark Bay 14 15 17	1

Date: Monday, August 12, 2013 Sheet 75 of 103



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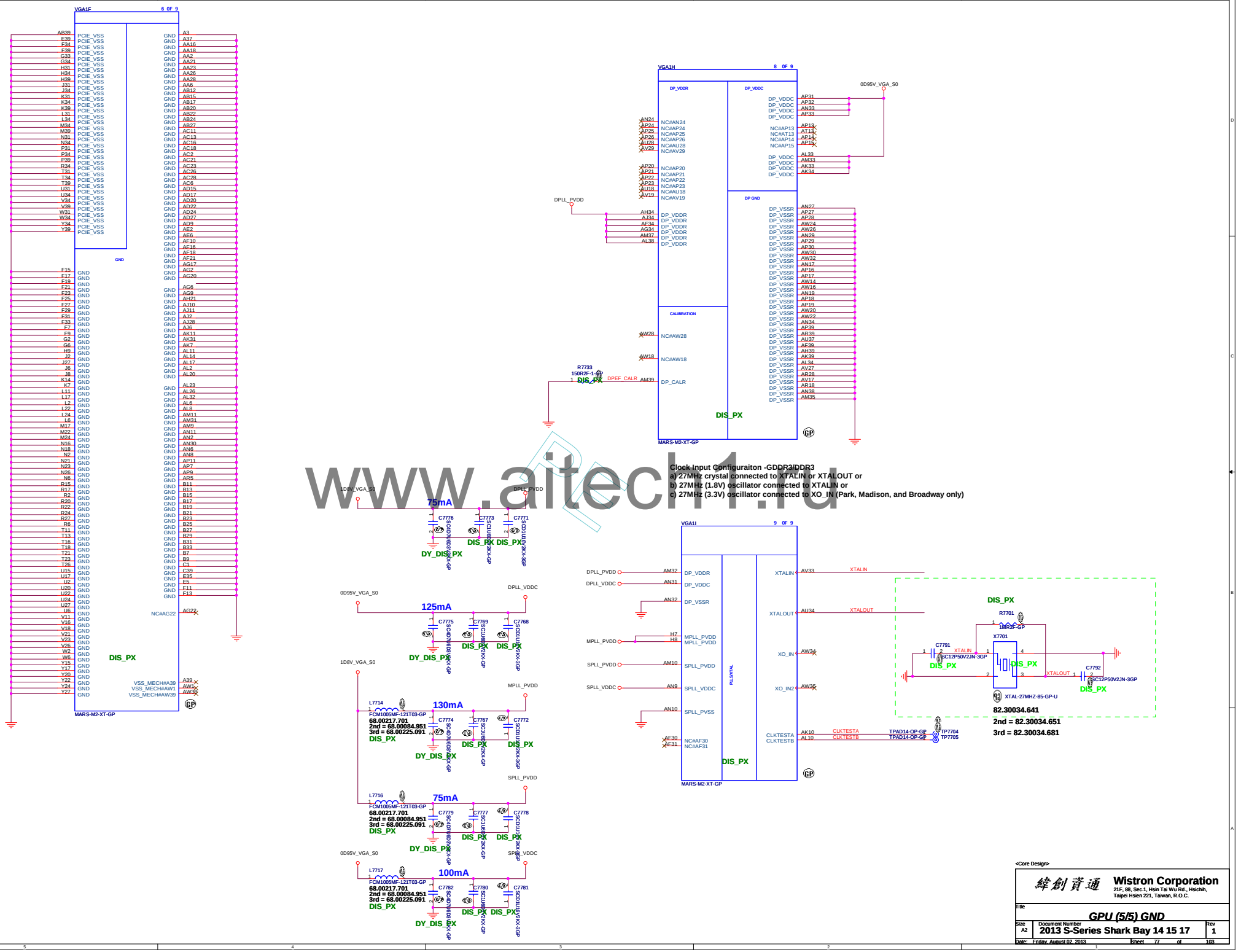

www.aitech1.ru

<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU (5/5) GND**

Size	Document Number	Rev
A2	2013 S-Series Shark Bay 14 15 17	1

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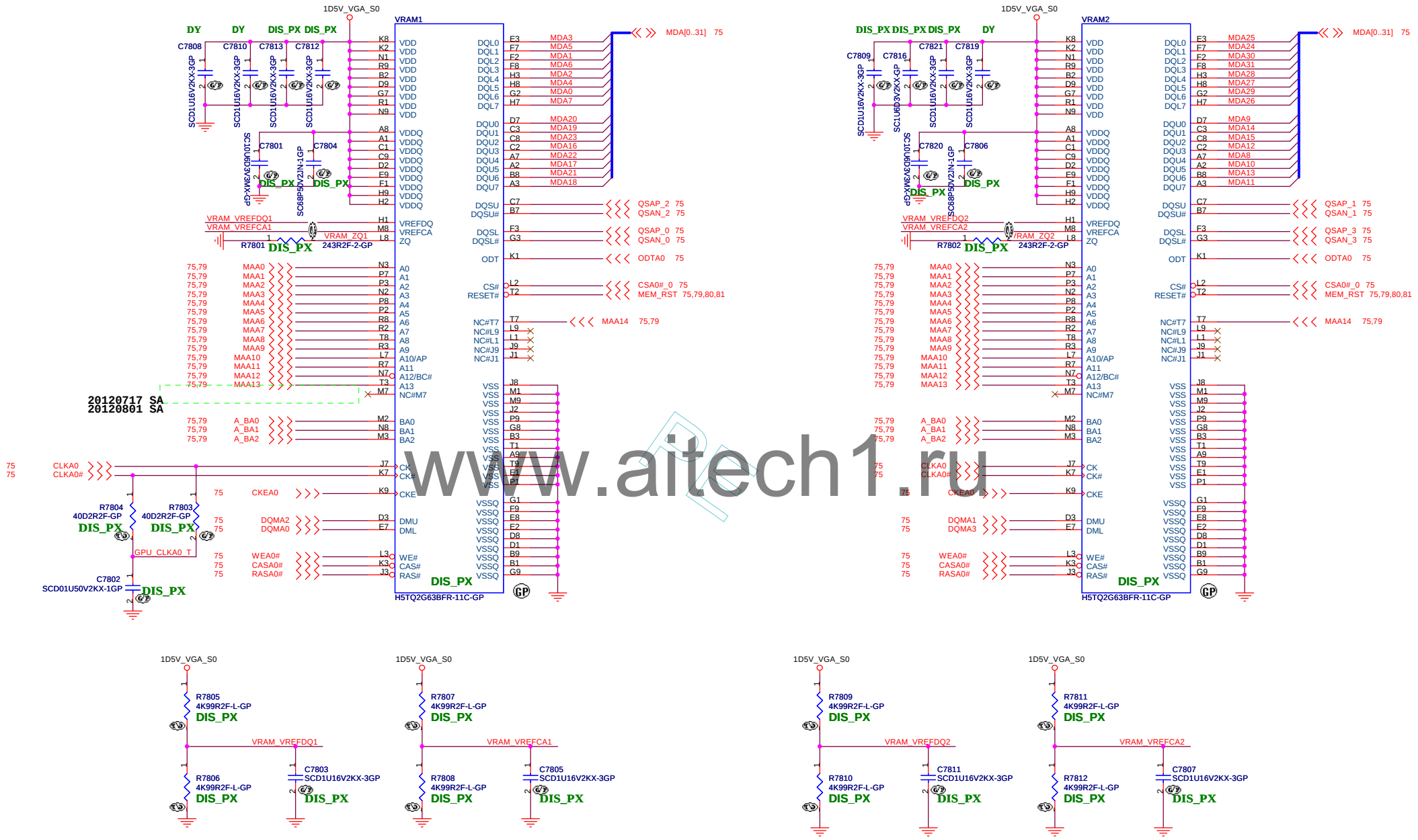

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VRAM1,2 (1/4)

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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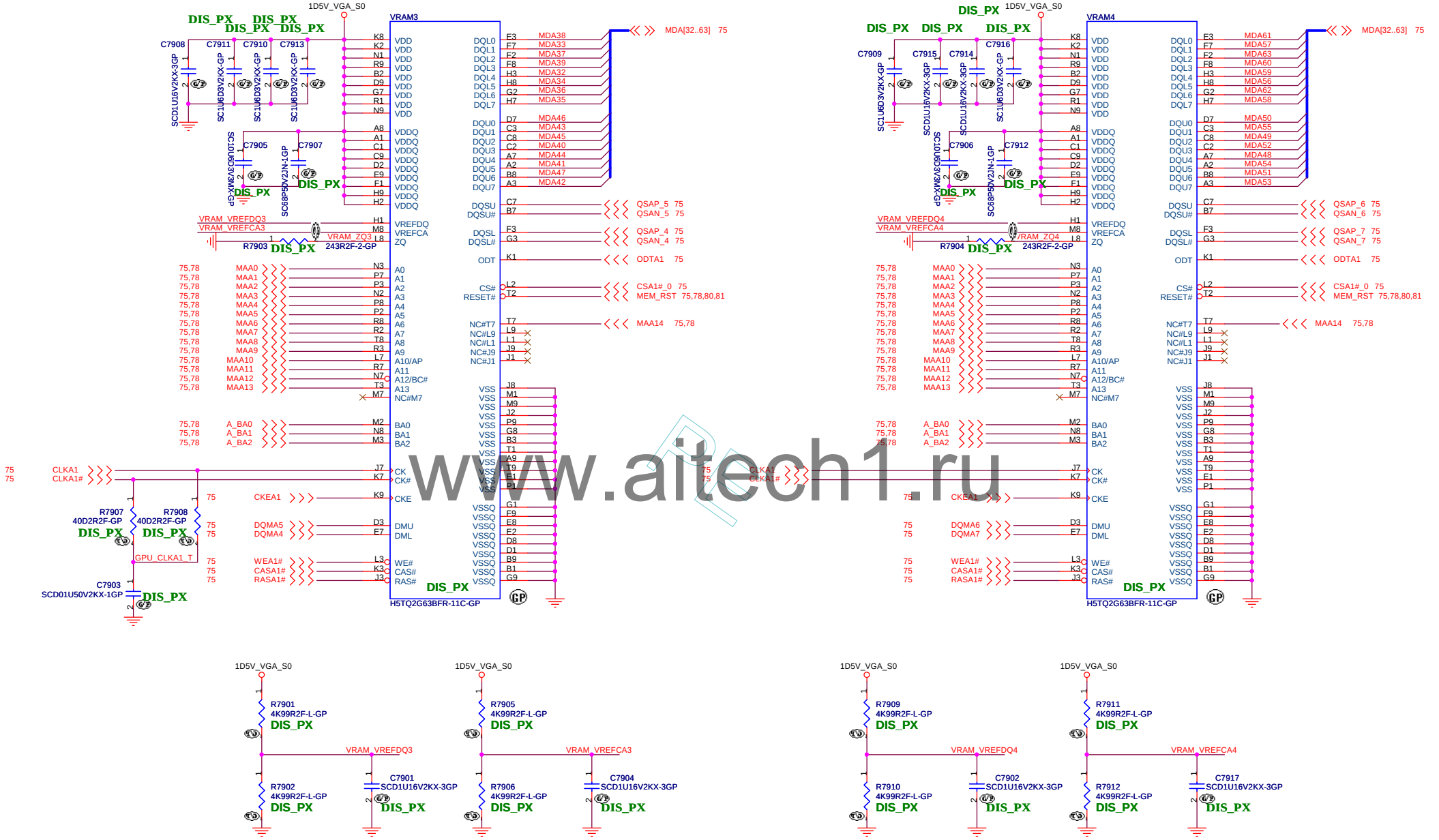

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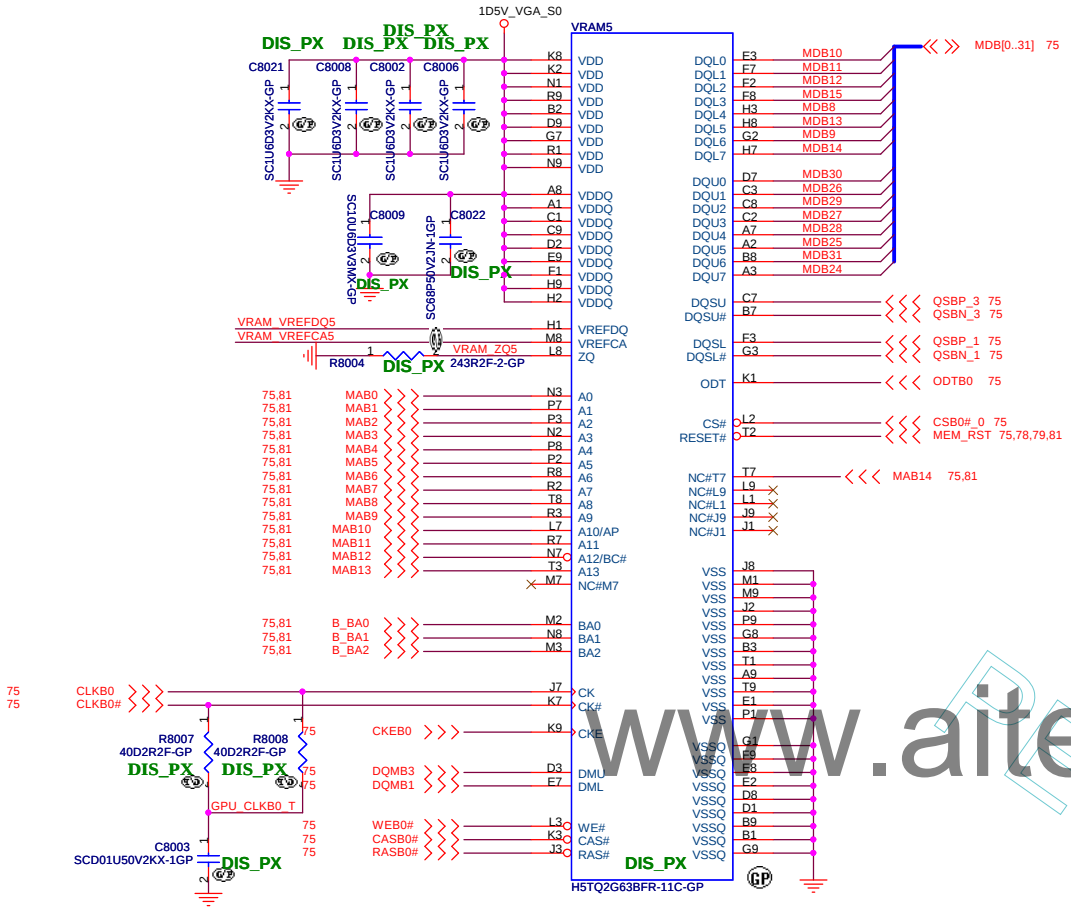
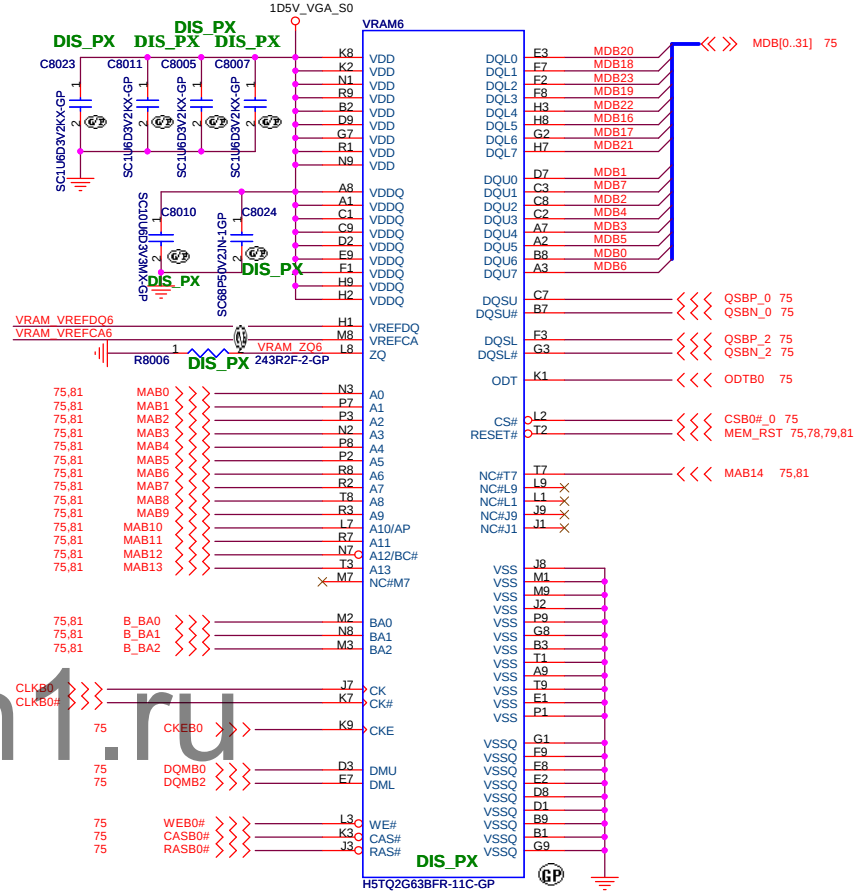
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

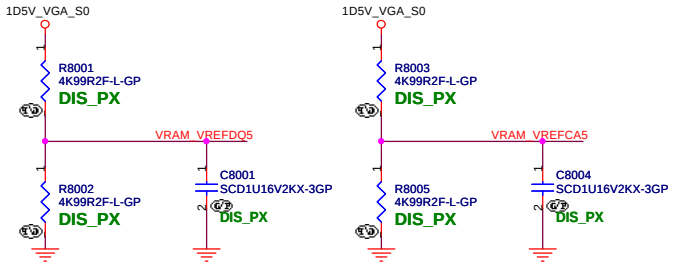
Title: VRAM3,4 (2/4)

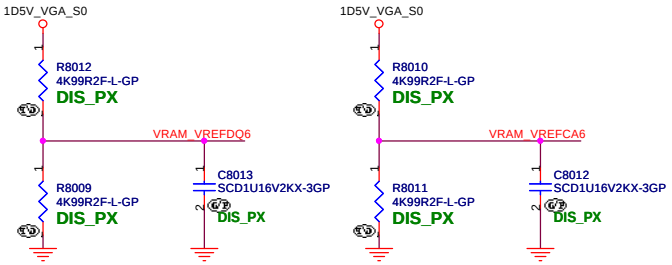
Size: A3 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

Date: Monday, August 12, 2013 | Sheet 79 of 103









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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VRAM5,6 (3/4)

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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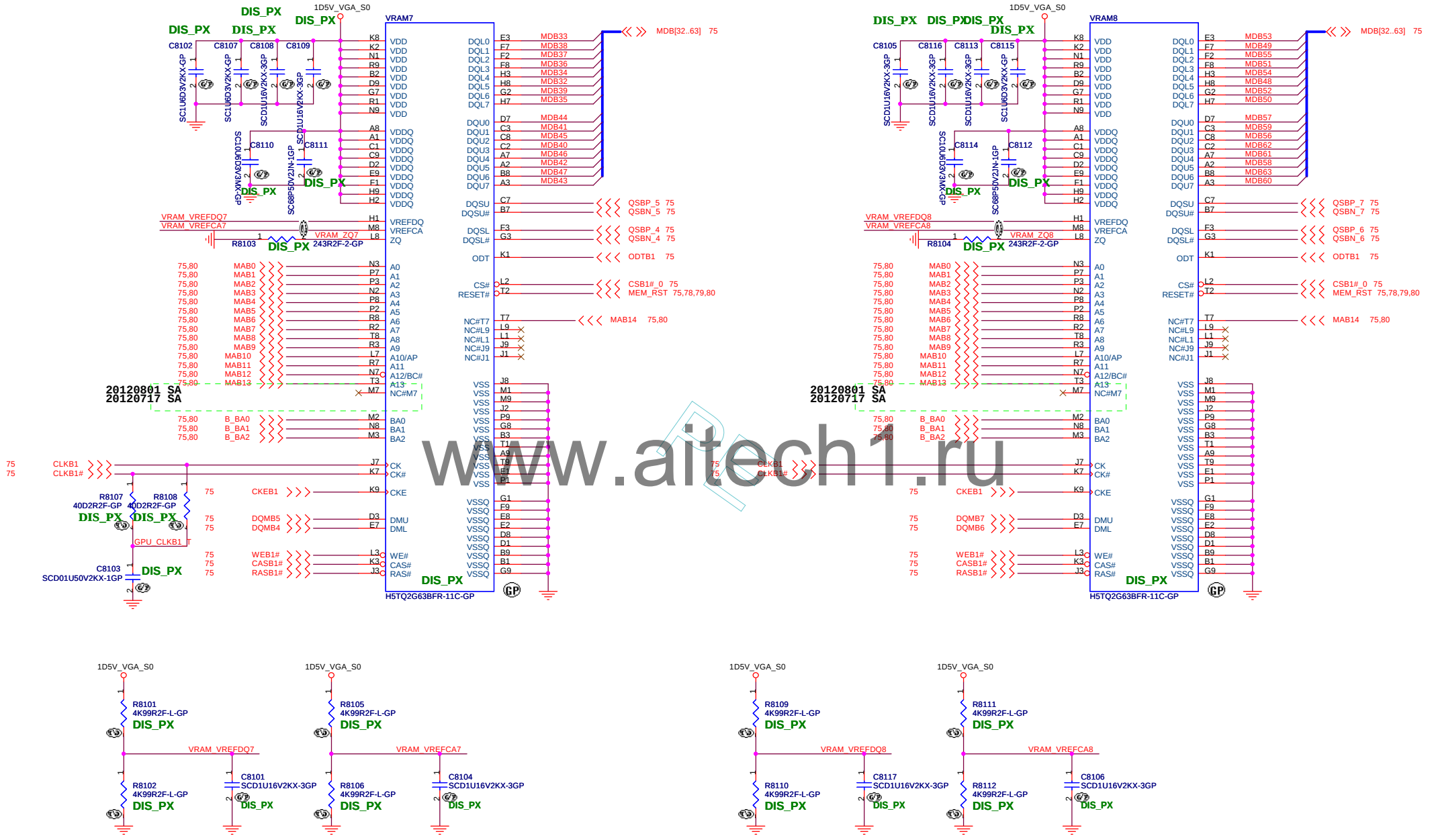

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VRAM7,8 (4/4)

Size: A3 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

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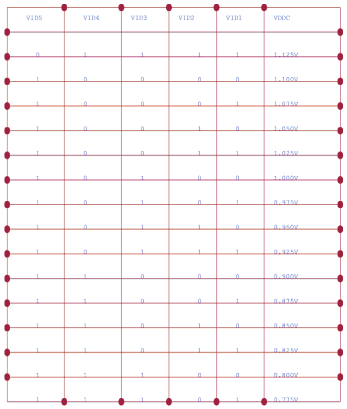
SSID = PWR.Plane.Regulator_vga_core

V-BOOT	VID0	VID1	VID2	VID3	VID4	VID5	VID6
0.85V	0	0	1	0	1	1	0



Design Current = 27A
OCP>55A

20130718 MV

20121011 Delete R8201 C8201

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA_CORE

Size: A2 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

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3D3V_VGA_S0 > VGA_CORE > 0D95V_VGA_S0 > 1D5V_VGA_S0 > 1D8V_VGA_S0

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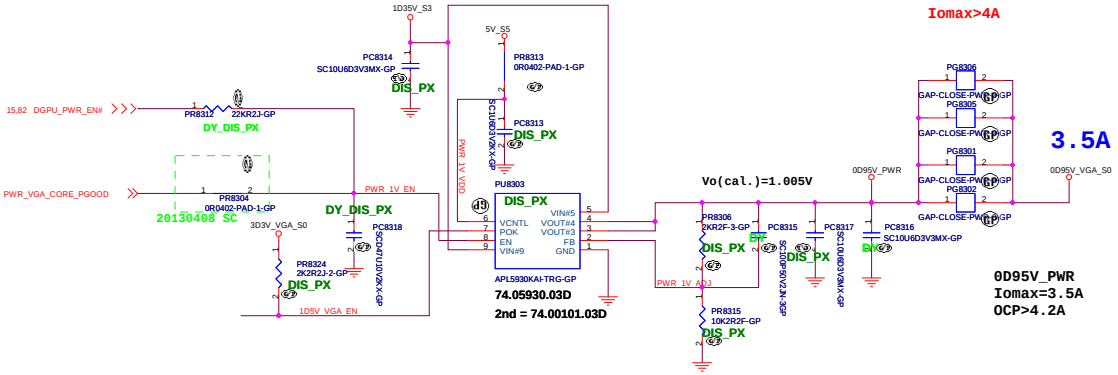
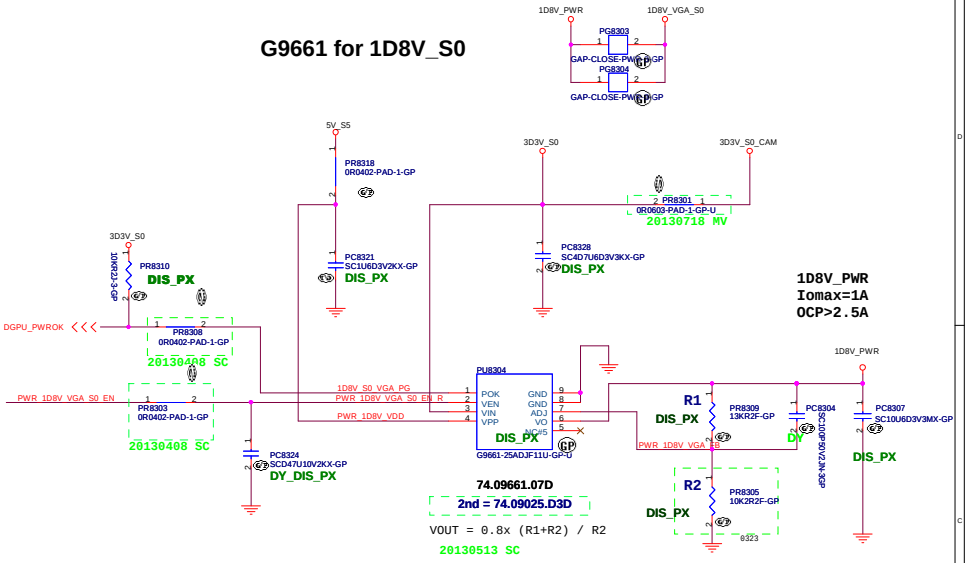
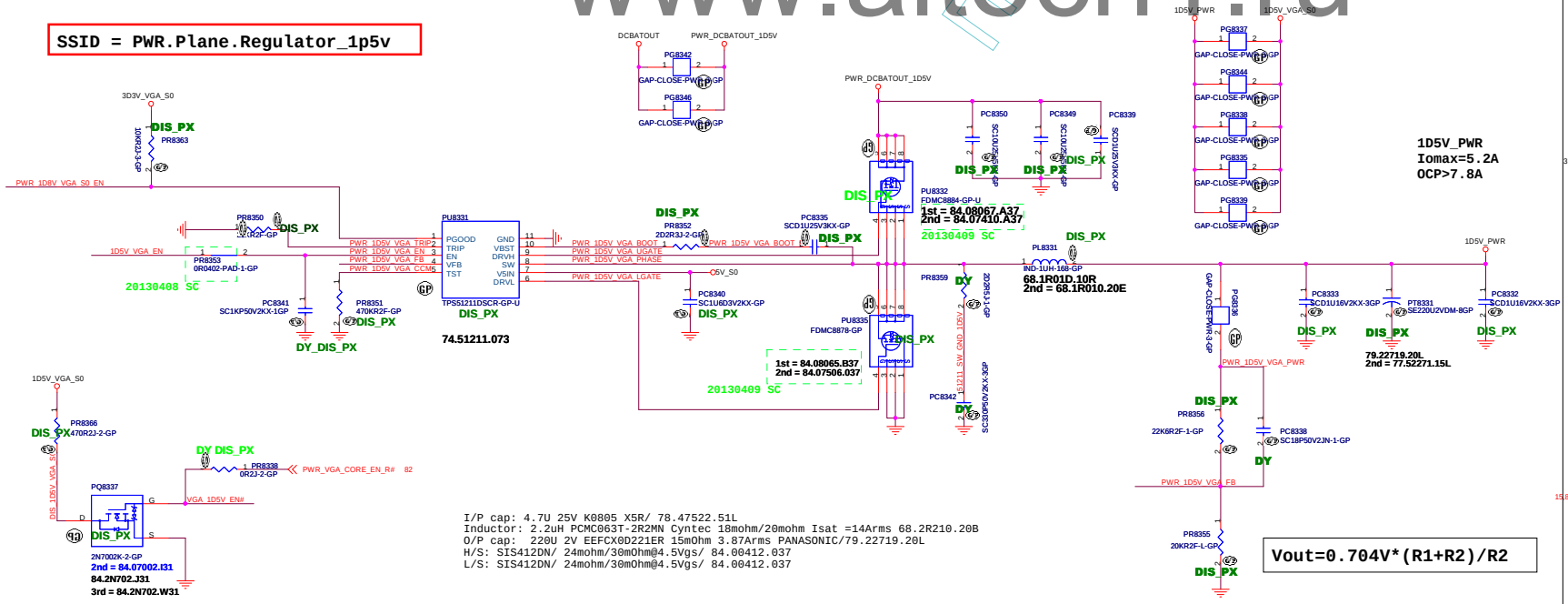
0D95V_S0



G9661 for 1D8V_S0



SSID = PWR.Plane.Regulator_1p5v



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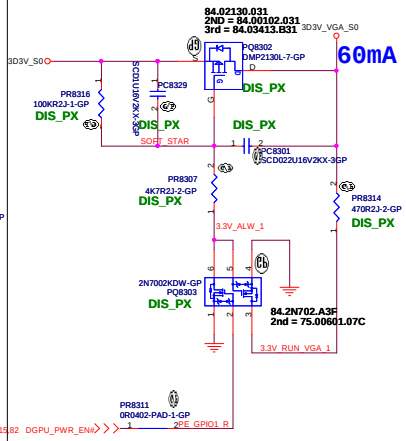

I/P cap: 4.7U 25V K0805 X5R/ 78.47522.51L
Inductor: 2.2uH PCMC063T-2R2MN Cyntec 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P cap: 220U 2V EEFCX0D221ER 15mOhm 3.87Arms PANASONIC/79.22719.20L
H/S: SIS412DN/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S: SIS412DN/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037

<Variant Name>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	DISCRETE VGA POWER	
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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU Memory(2/5)*

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_DP/LVDS/CRT/GPIO(3/5)

Size: A2 | Document Number: 2013 S-Series Shark Bay 14/15/17 | Rev:

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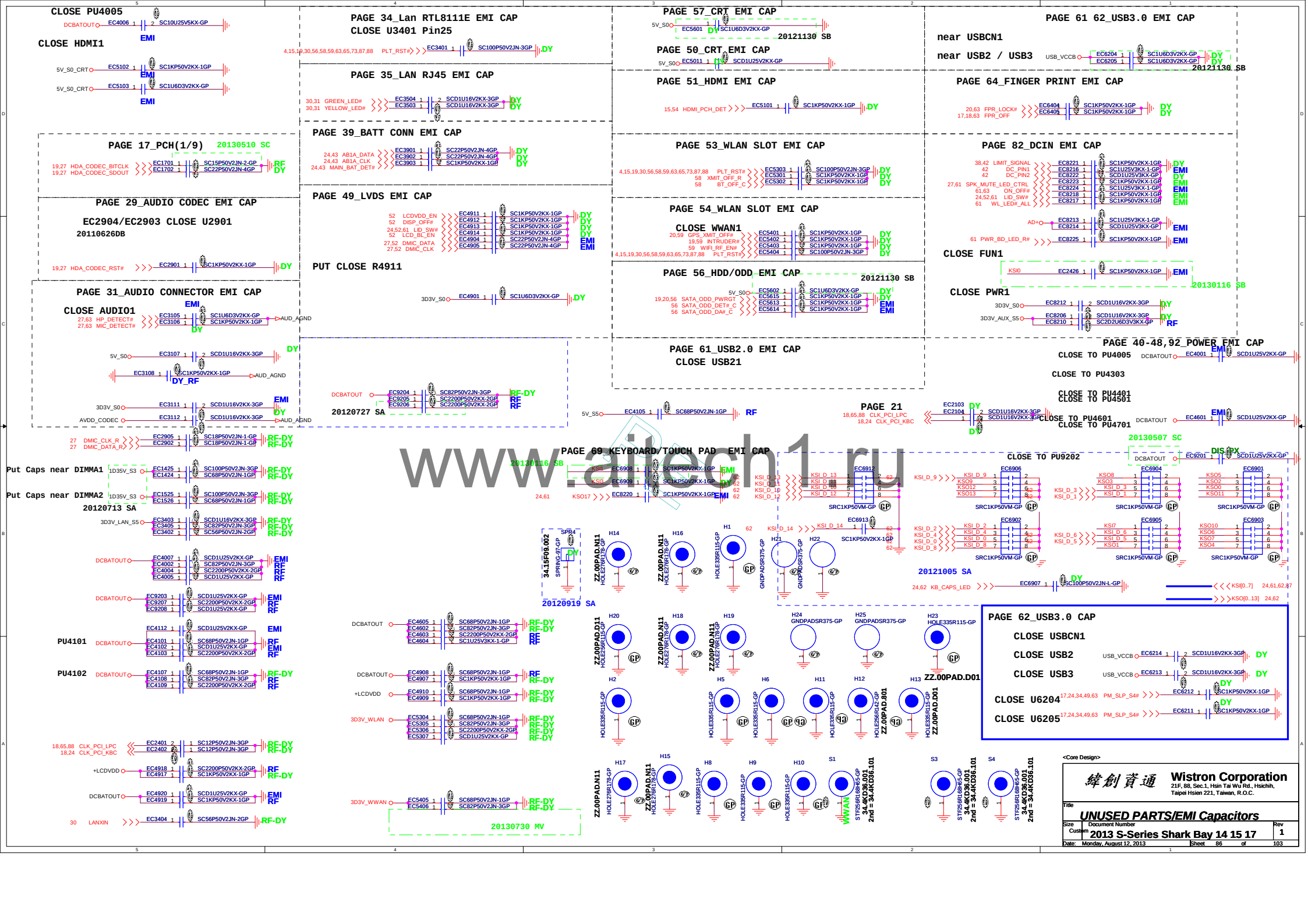

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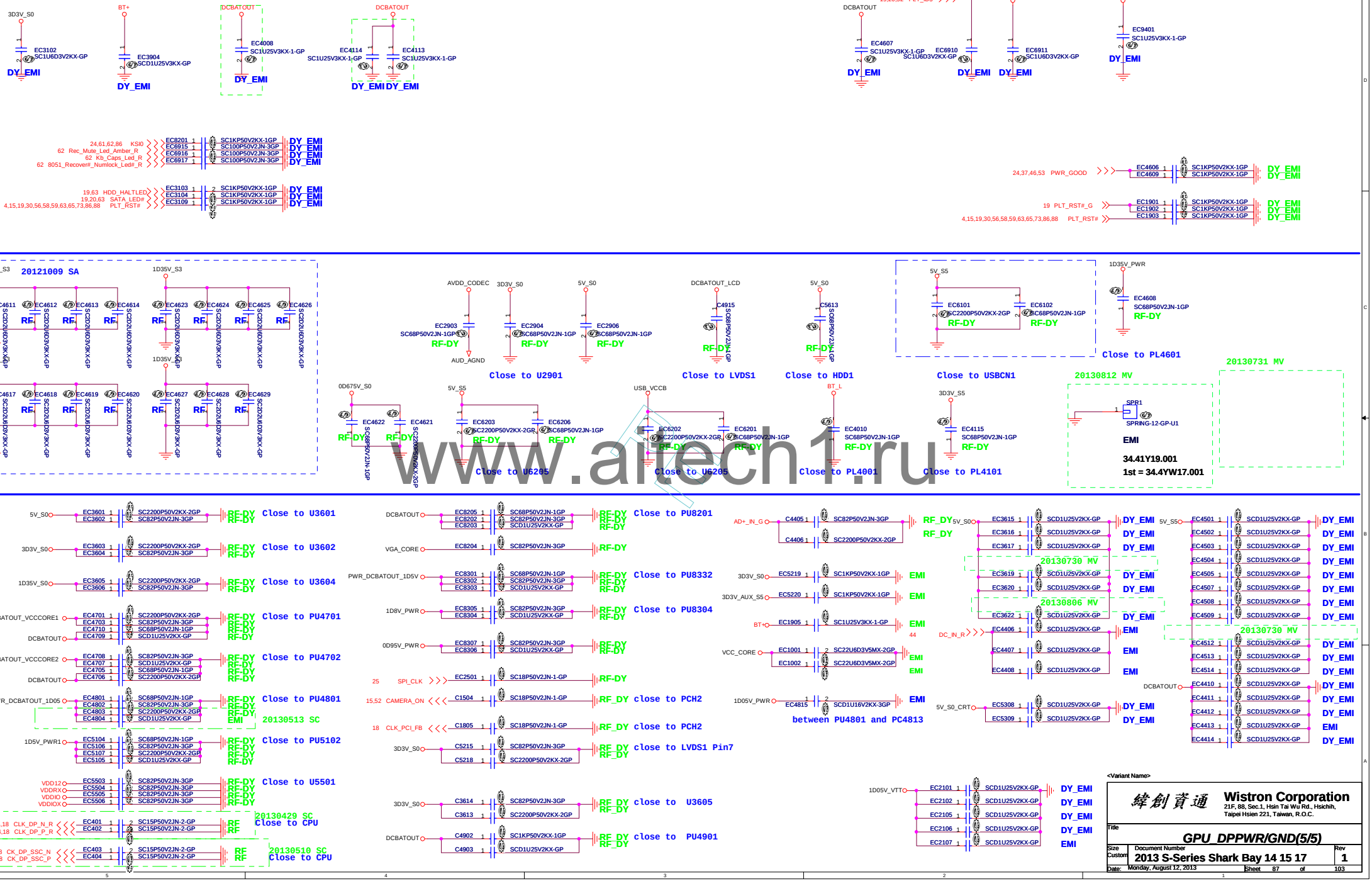
EMI Caps



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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_DPPWR/GND(5/5)

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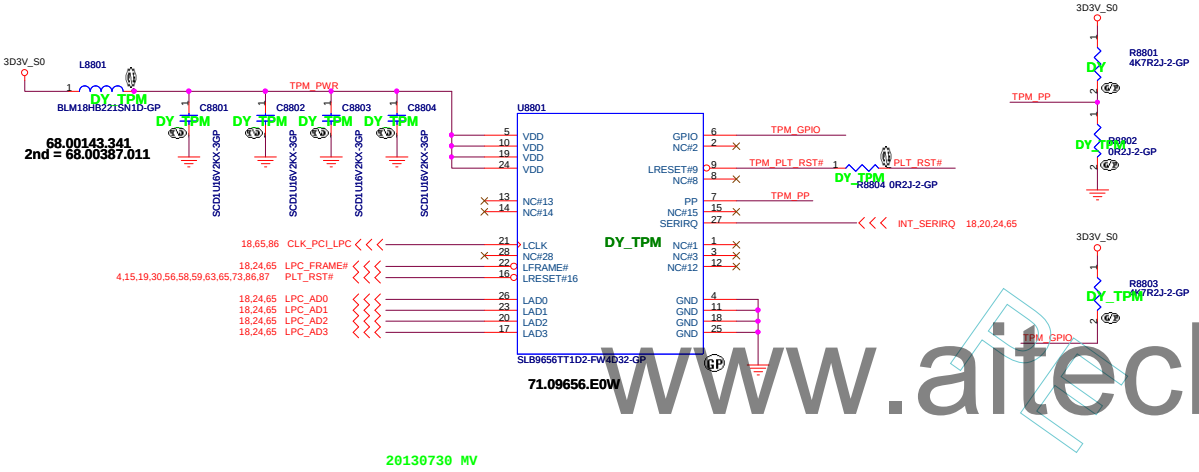

20130730 MV

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPM

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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Finger Print Conn***

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<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

GPU-VRAM5,6 (3/4)

Size	Document Number	Rev
A2	2013 S-Series Shark Bay 14/15 17	1.0

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM7,8 (4/4)

Size: A2 | Document Number: 2013 S-Series Shark Bay 14/15 17 | Rev:

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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***NCP3218 VGACORE25W***

Size: A2 | Document Number: **2013 S-Series Shark Bay 14/15 17** | Rev: 1

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DISCRETE VGA POWER***

Size	Document Number	Rev
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<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1.1

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<Core Design>

緯創資通 Wistron Corporation
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Title: Reserved

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Shark Bay SV

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU XDP***

Size	Document Number	Rev
A3	**2013 S-Series Shark Bay 14 15 17**	1

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
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<Core Design>

緯創資通 **Wistron Corporation**

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Title

Change History

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14"15 17	1

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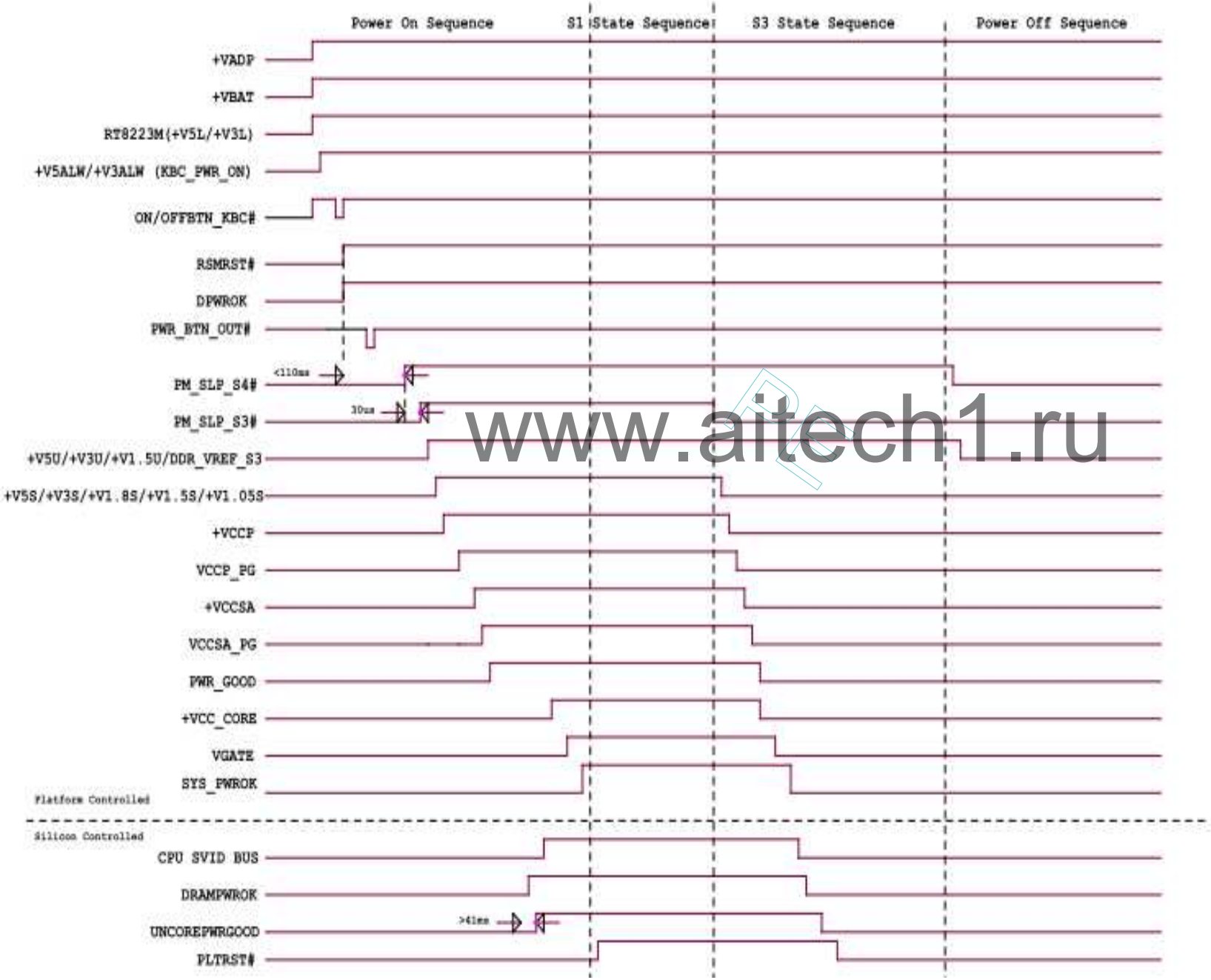
S-Series Power Sequence and Reset Signal Timing



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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power Sequence***

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A3	2013 S-Series Shark Bay 14/15 17	1

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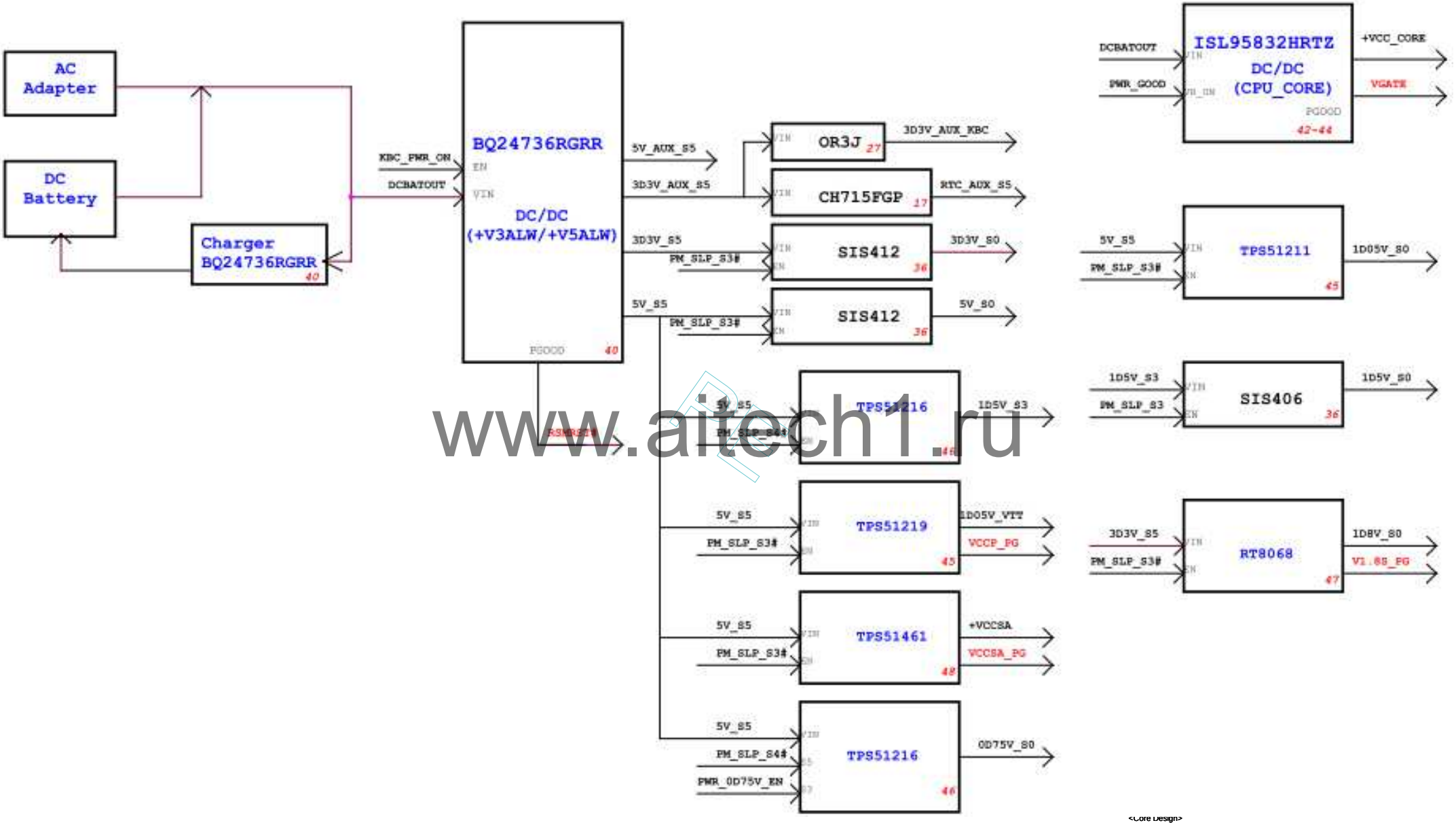
S-Series POWER BLOCK DIAGRAM



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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Block Diagram

Size	Document Number	Rev
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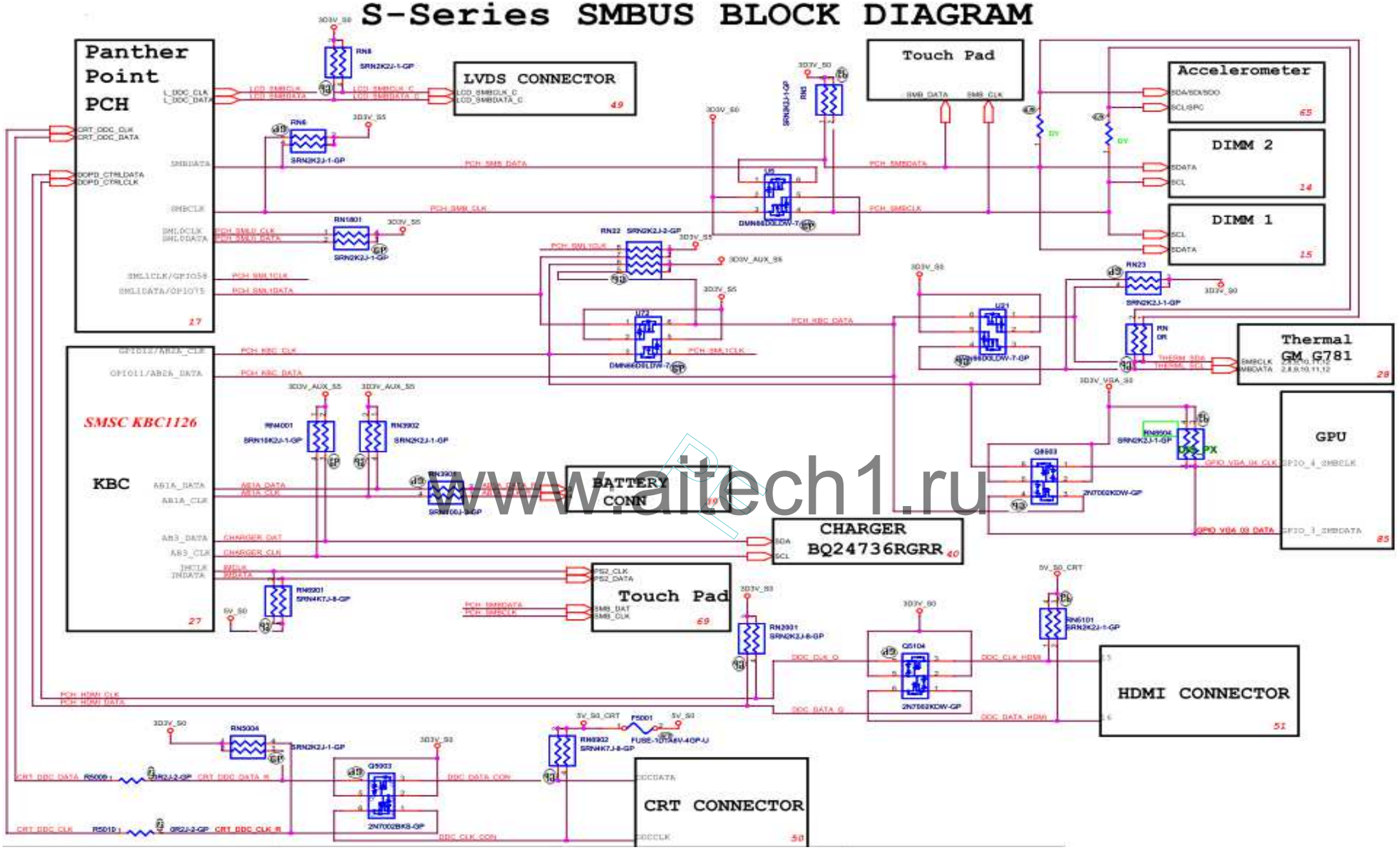
S-Series SMBUS BLOCK DIAGRAM



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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: ***SMBUS Block Diagram***

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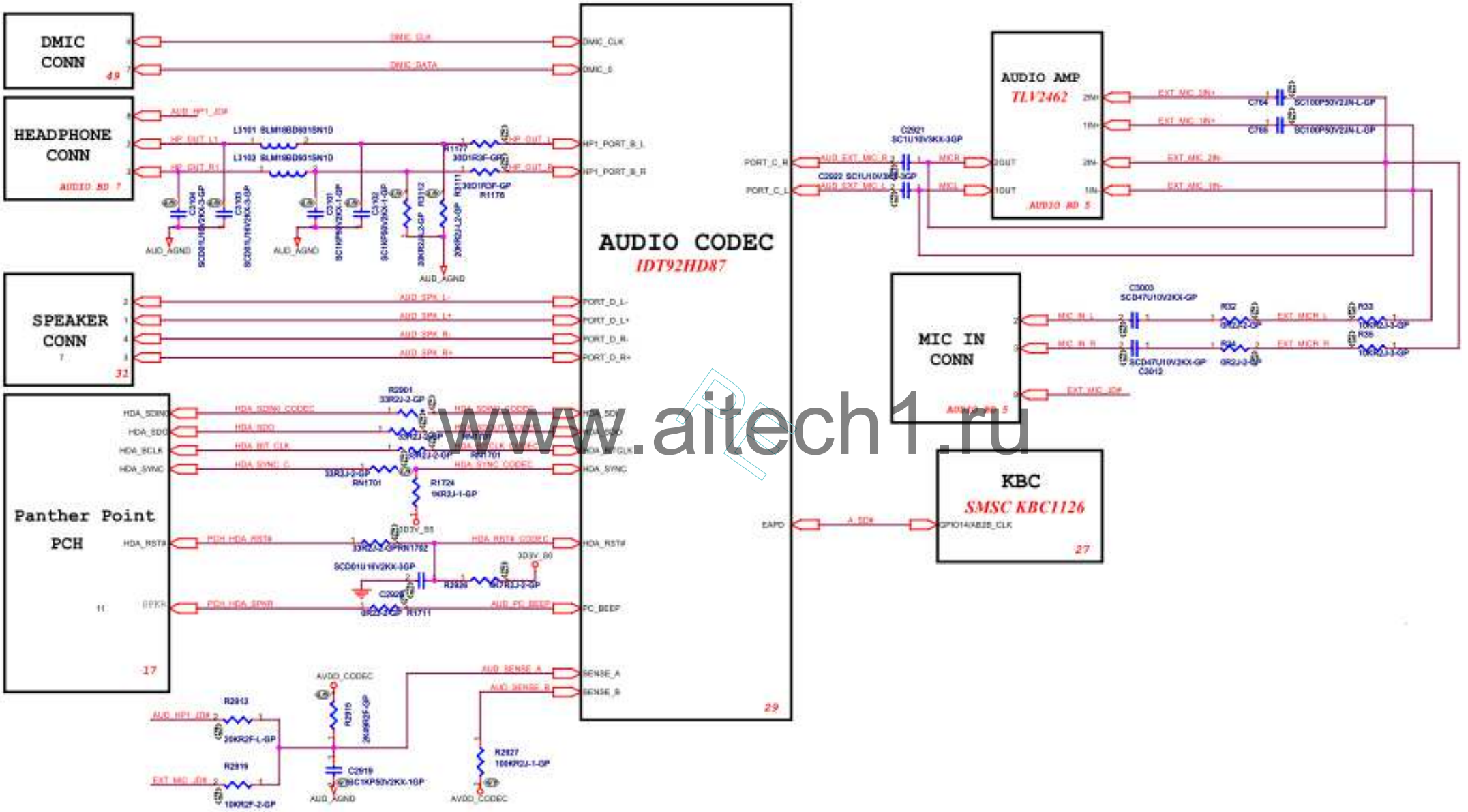
S-Series AUDIO BLOCK DIAGRAM



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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Audio Block Diagram

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A3	2013 S-Series Shark Bay 14/15 17	1

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *mSATA*

Size: A3 | Document Number: 2013 S-Series Shark Bay 14"15 17 | Rev: 1

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